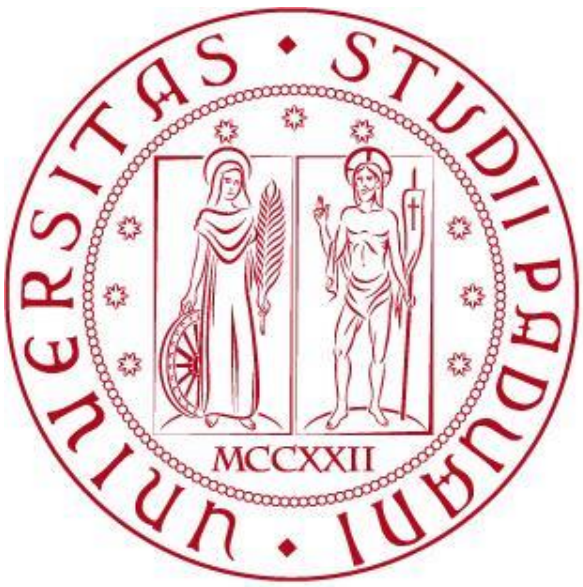

UNIVERSITÀ
DEGLI STUDI
DI PADOVA

NOTES OF

ELECTRONICS

Op. Amplifiers, Diodes, MOSFETs, IC amplifiers and CMOS.

(Version 07/06/2019)

Edited by:
Stefano Ivancich

Table of Content

This document was written by students with no intention of replacing university materials. It is a useful tool for the study of the subject but does not guarantee an equally exhaustive and complete preparation as the material recommended by the University.
The purpose of this document is to summarize the fundamental concepts of the notes taken during the lesson, rewritten, corrected and completed by referring to the slides and the textbook: "*Microelectronic Circuits Sedra Smith 7th Edition - Chapters 1-9 and 14*" to be used in the design of electronic circuits as a "practical and quick" manual to consult. There are no examples and detailed explanations, for these please refer to the cited texts and slides.

If you find errors, please report them here:
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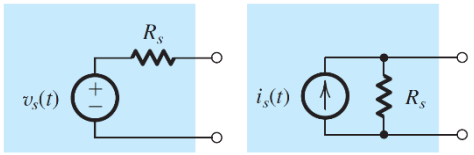
The document will be updated as soon as possible.

1.Signals and Amplifiers

1.1. Signals

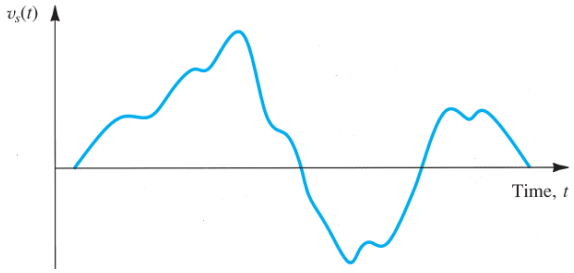
To extract required information from a set of signals, a signal must first be converted into an electrical signal by transducers, then we apply signal processing.
we assume that the signals of interest already exist in the electrical domain and represent them by one of the two equivalent forms:

- a voltage source $v_s(t)$ having a source resistance R_s.
- or a current source $i_s(t)$ having a source resistance R_s.

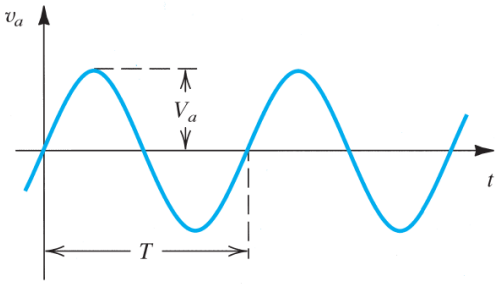


The two representations are related by $v_s(t) = R_s i_s(t)$

A signal is a time-varying quantity that can be represented by a graph:



Frequency Spectrum of Signals: is a description of signals obtained through Fourier series and Fourier transform, they can represent a voltage signal $v_s(t)$ or a current signal $i_s(t)$ as the sum of sine-wave signals.



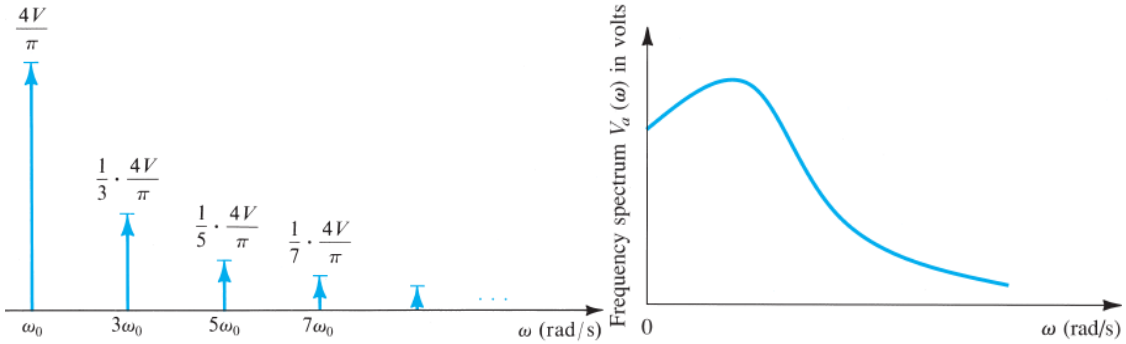
$$v_a(t) = V_a \sin \omega t$$

$V_a\ [V]$ denotes the peak value or amplitude
$\omega = 2\pi f\ [rad/s]$ denotes the angular frequency
$f = \frac{1}{T}\ [Hz]$ is the frequency
$T\ [s]$ is the period

It is common to express the amplitude in terms of its root-mean-square (rms) $= V_a/\sqrt{2}$

Fourier series is utilized in the special case of a signal that is a periodic function of time.
Fourier transform is more general and can be used to obtain the frequency spectrum of a signal whose waveform is an arbitrary function of time.

Periodic signals spectrum consists of discrete frequencies.
Nonperiodic signal spectrum contains in general all possible frequencies.

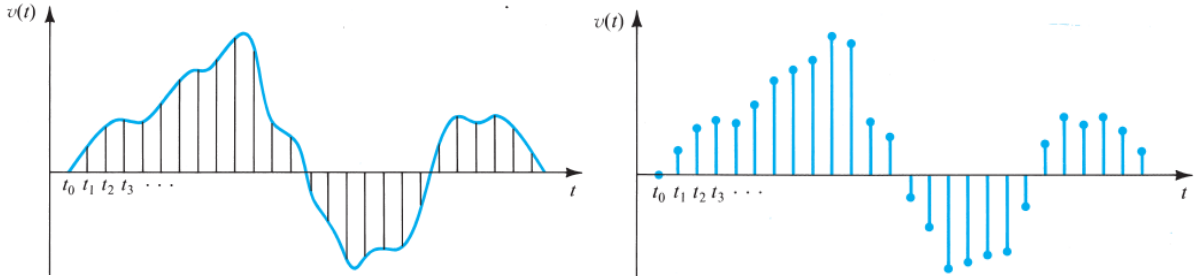


1.2. Analog and Digital Signals

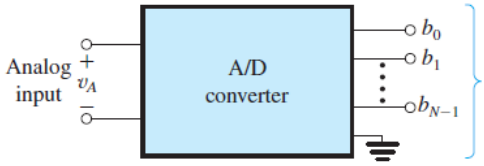
Analog signal: the magnitude can take on any value.
The vast majority of signals in the world around us are analog. Electronic circuits that process such signals are known as analog circuits.
Digital signal: the magnitude at each instant of time is represented by a sequence of numbers.

Signals can be converted from analog to digital:

- using a process called **sampling** which measure the signal at equal intervals along the time axis,
- then representing the magnitude of each of the signal samples by a number having a finite number of digits.



The **binary** number system is the simplest possible digital signals and circuits. Takes on one of only two possible values, denoted 0 and 1. So two voltage levels which can be labeled low and high.
If we use N binary digits (bits) to represent each sample of the analog signal



$$D = b_0 2^0 + \cdots + b_{N-1} 2^{N-1}$$

$b_0, b_1, \ldots, b_{N-1}$, denote the N bits, have values of 0 or 1.
b_0 is the least significant bit (LSB)
b_{N-1} is the most significant bit (MSB)
Such a representation quantizes the analog sample into one of 2^N levels.

Once the signal is in digital form, it can be processed using digital circuits.

1.3. Amplifiers

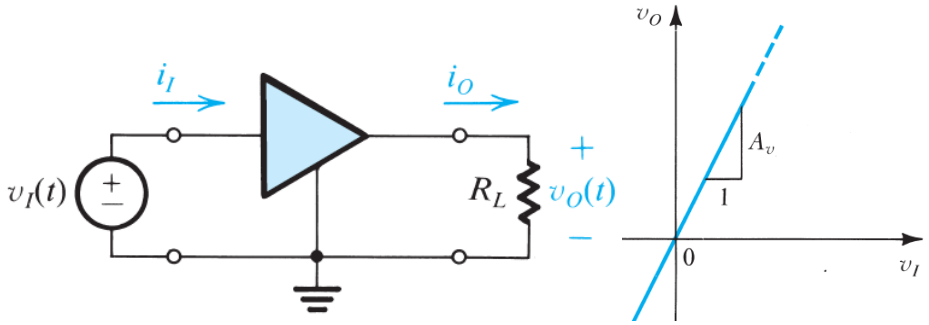
Signal Amplification: is simplest signal-processing task, used because transducers provide signals that are in the microvolt (µV) or millivolt (mV), so too small for reliable processing.

Linearity: during amplification information contained in the signal is not changed and no new information is introduced.
Distortion: when amplification introduces any change in the waveform.

Linear amplifier:

$$v_o(t) = Av_i(t)$$

A is a constant called amplifier gain

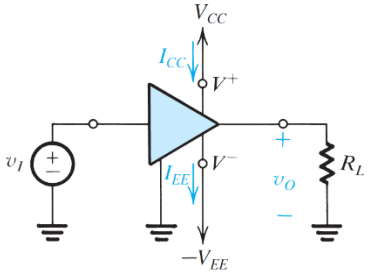


- Voltage gain $A_v = \frac{v_O}{v_I}$
- Power gain $A_p \equiv \frac{load\ power\ P_L}{input\ power\ P_I} = \frac{v_O i_O}{v_I i_I}$
- Current gain $A_i \equiv \frac{i_O}{I_i}$
- $A_p = A_v A_i$

Expressing Gain in Decibels:

- Voltage gain in decibels $= 20 \log|A_v|\ dB$
- Current gain in decibels $= 20 \log|A_i|\ dB$
- Power gain in decibels $= 10 \log|A_p|\ dB$

The Amplifier Power Supplies: amplifiers need dc power supplies for their operation.
Amplifier usually requires two dc sources: one positive of value VCC and one negative of value VEE.



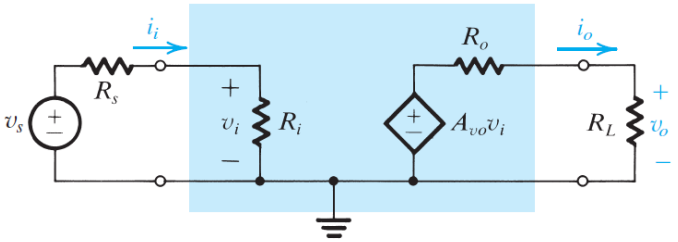
Power delivered to the amplifier $P_{dc} = V_{CC}I_{CC} + V_{EE}I_{EE}$
Power-balance equation: $P_{dc} + P_I = P_L + P_{dissipated}$
Amplifier power efficiency $\eta \equiv \frac{P_L}{P_{dc}} \times 100$

Some amplifiers require only one power supply.

Amplifier Saturation: the output voltage cannot exceed a specified positive limit and cannot decrease below a specified negative limit. Saturation levels are denoted L_+ and L_-
The input signal must be kept within $\frac{L_-}{A_v} \le v_i \le \frac{L_+}{A_v}$

1.4. Circuit Models for Amplifiers

Voltage Amplifier:



$$v_o = A_{vo} v_i \frac{R_L}{R_L + R_o}$$

$$A_v = \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o}$$

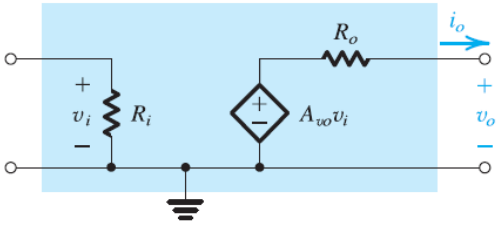
$$R_o = 0 \ll R_L \quad R_i = \infty \gg R_s$$

Overall Voltage gain: $\frac{v_o}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o}$

Buffer amplifier: Sometimes we are interested in power gain, for instance when $R_s \gg R_L$, so we will design the amplifier to have $R_i \gg R_s$, $R_o \ll R_L$ and **voltage gain = 1**.

Cascaded Amplifiers: we often need to design the amplifier as a cascade of two or more stages. The stages are usually not identical, each is designed to serve a specific purpose.

Voltage Amplifier

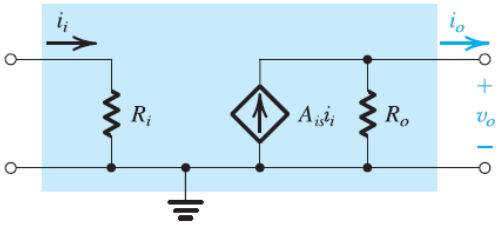


Open-Circuit Voltage Gain

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{i_o=0} \text{(V/V)}$$

$R_i = \infty$
$R_o = 0$

Current Amplifier

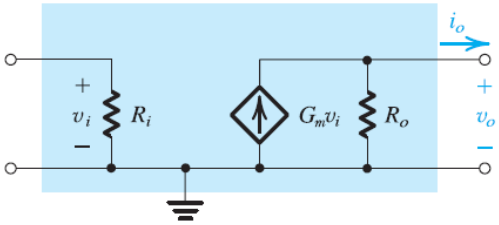


Short-Circuit Current Gain

$$A_{is} \equiv \left.\frac{i_o}{i_i}\right|_{v_o=0} \text{(A/A)}$$

$R_i = 0$
$R_o = \infty$

Transconductance Amplifier

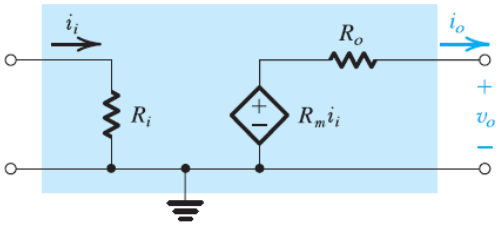


Short-Circuit Transconductance

$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{v_o=0} \text{(A/V)}$$

$R_i = \infty$
$R_o = \infty$

Transresistance Amplifier



Open-Circuit Transresistance

$$R_m \equiv \left.\frac{v_o}{i_i}\right|_{i_o=0} \text{(V/A)}$$

$R_i = 0$
$R_o = 0$

Relationships between the Four Amplifier Models:

$$A_{vo} = A_{is} \frac{R_o}{R_i} \qquad A_{vo} = G_m R_o \qquad A_{vo} = \frac{R_m}{R_i}$$

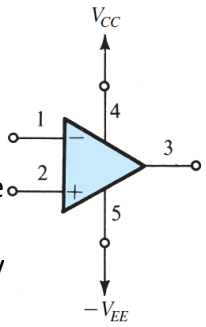
Determining R_i and R_o:

- R_i : applying an input voltage v_i and measuring the input current i_i. $R_i = v_i / i_i$
- R_o: eliminating the input signal source and applying a voltage signal v_x to the output of the amplifier. $R_o = v_x / i_x$

Unilateral Models: signal flow is unidirectional, from input to output.

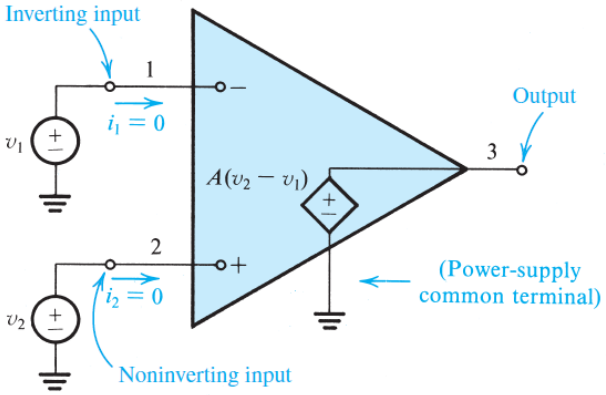
2. Operational Amplifiers

2.1. The Ideal Op Amp



Terminals:

- Two input terminals: "-" is the **inverting input**, "+" is the **noninverting input**
- One output terminal
- Two terminals connected to a positive voltage V_{CC} and a negative voltage $-V_{EE}$
- May have other terminals for specific purposes, like for frequency compensation and offset nulling.



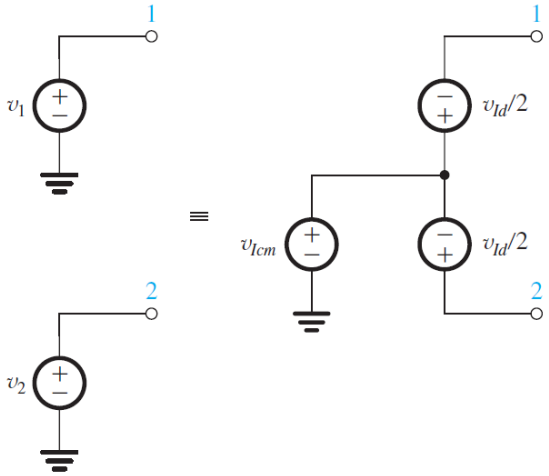
Characteristics:

- $\boldsymbol{v_o = A(v_+ - v_-)}$
- The input impedance of an ideal op amp is infinite. So there is **no input current**.
- $R_o = 0$. So $v_o = A(v_+ - v_-)$ always.
- Infinite Common mode rejection property: if $v_+ = v_-$ then $v_o = 0$
- Amplifies both DC and signal
- Have infinite bandwidth. Amplifies signals in all frequencies
- Open loop gain $A = \infty$

In almost all applications the op amp will not be used alone in a so-called open-loop configuration. Rather, we will use other components to apply feedback to close the loop around the op amp.

Differential input signal: $v_{Id} = v_+ - v_-$

Common-mode input signal: $v_{Icm} = \frac{1}{2}(v_+ + v_-)$



2.2. The Inverting Configuration

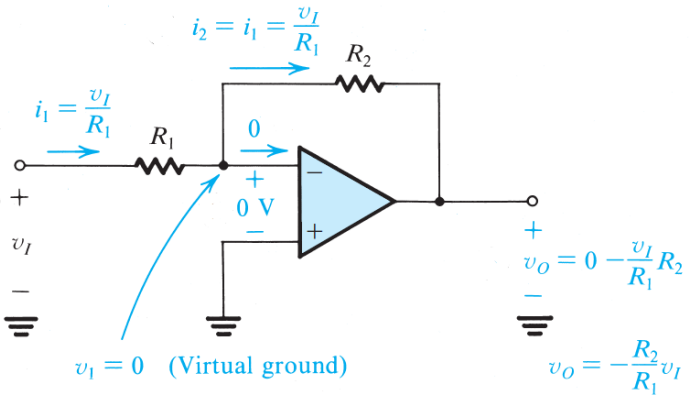
Closed-loop gain $A_v \equiv \frac{v_o}{v_i} = -\frac{R_2}{R_1}$

Virtual short circuit: whatever voltage is at 2 will automatically appear at 1 because of the infinite gain A. Terminal 2 is connected to ground so $v_+ = v_- = 0$

Input Resistance $R_i = R_1$

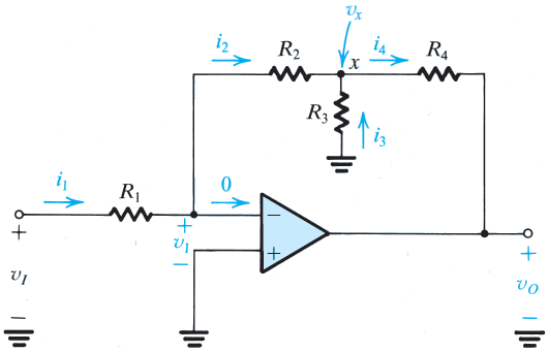
Output Resistance $R_o = 0$

If A is not infinite: $A_v = \frac{-R_2/R_1}{1+\left(1+\frac{R_2}{R_1}\right)/A}$



Problem: The amplifier input resistance forms a voltage divider with the resistance of the source that feeds the amplifier. To avoid the loss of signal strength, voltage amplifiers are required to have high input resistance. To make R_i high we should select a high value for R_1.
If the required gain R2/R1 is also high, then R2 could become impractically large.

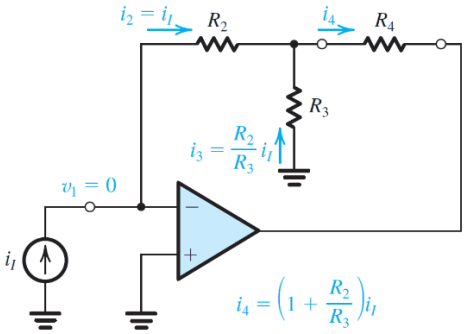
Solution: circuit with "T" feedback.



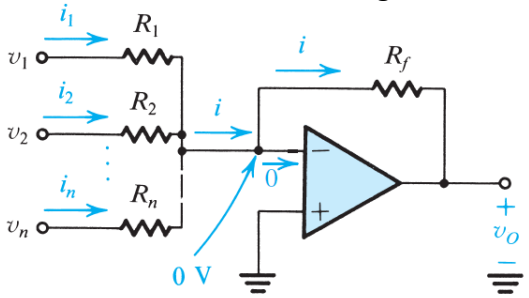
$$G = -\frac{R_2}{R_1}\left(1 + \frac{R_4}{R_2} + \frac{R_4}{R_3}\right)$$

We can increase R_1 and compensate the gain loss increasing R_4/R_3

This configuration can also be used as a current amplifier, using R_4 as load.

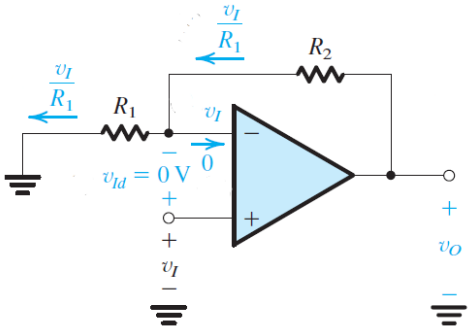


Application: The Weighted Summer. All the summing coefficients must be of the same sign.



$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

2.3. The Non-Inverting Configuration



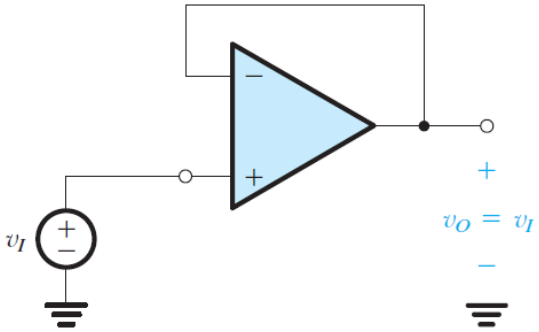
Closed-loop gain $\boldsymbol{A_v \equiv \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1}}$

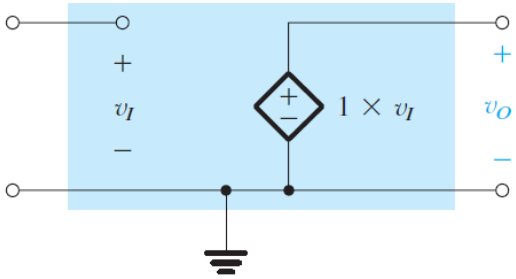
Input Resistance $R_i = \infty$

Output Resistance $R_o = 0$

If A is not infinite: $A_v = \frac{1+R_2/R_1}{1+\left(1+\frac{R_2}{R_1}\right)/A}$

Application: The Voltage Follower. Buffer amplifier (due to infinite Ri) with $R_2 = 0, R_1 = \infty$





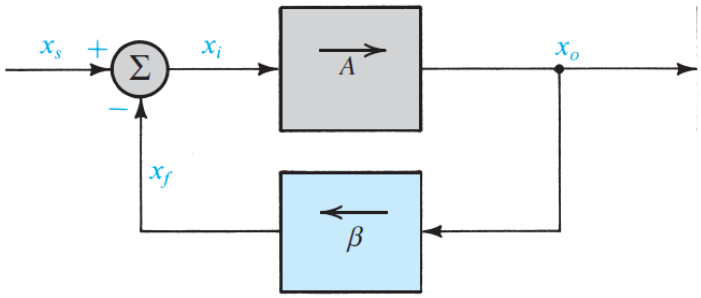
2.3.1. Feedback

Feedback can be either negative or positive.

Negative feedback is used to: Desensitize the gain, reduce nonlinear distortion, Reduce the effect of noise, Control the input and output resistances, Extend the bandwidth.

negative feedback reduces the signal that appears at the input of the basic amplifier.

Feedback network does not load the amplifier input.



Open-loop gain A

Feedback gain β

Loop gain $A\beta$

Amount of feedback $1 + A\beta$

Closed-loop gain $A_f = \frac{A}{1+A\beta}$

For large loop gain: $A_f \cong \frac{1}{\beta}$

The noninverting op-amp configuration provides a direct implementation of the feedback loop.

$$\boldsymbol{A_f = 1 + \frac{R_2}{R_1}}$$

$$\boldsymbol{\beta = \frac{R_1}{R_1 + R_2}}$$

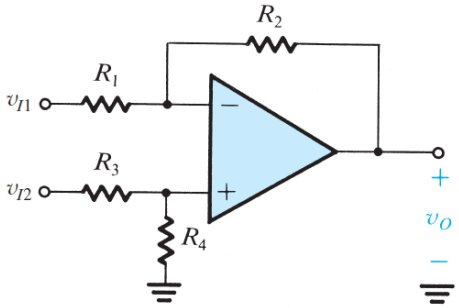
2.4. Difference Amplifiers

Amplifies the difference between the input signals.

$$\boldsymbol{v_o = A_d v_{id} + A_{cm} v_{icm}}$$

$$v_{Id} = v_2 - v_1 \quad v_{Icm} = \frac{1}{2}(v_2 + v_1)$$

$\boldsymbol{A_d}$ is the **differential gain** and $\boldsymbol{A_{cm}}$ is common-mode gain. $A_d \gg A_{cm}$



$\boldsymbol{v_o = \frac{R_2}{R_1}(v_{i_2} - v_{i1})}$ with $R_3 = R_1$ e $R_4 = R_2$

Otherwise: $A_{cm} = \left(\frac{R_4}{R_4+R_3}\right)\left(1 - \frac{R_2}{R_1}\frac{R_3}{R_4}\right)$

Differential input resistance $\boldsymbol{R_{id} = 2R_1}$

Is usually required to have a high input resistance.

Common-mode rejection ratio: $\boldsymbol{\text{CMRR}|_{\text{dB}} = 20 \log \frac{|A_d|}{|A_{cm}|}}$

measure the efficacy of the differential amplifier.

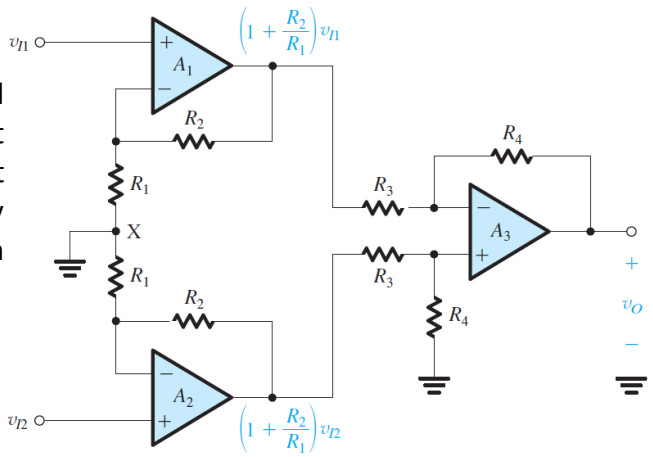
Problems of this circuit:

- if the amplifier is required to have a large differential gain (R2/R1), then R1 of necessity will be relatively small and the input resistance R_{id} will be correspondingly low.
- it is not easy to vary the differential gain of the amplifier

Solution: Instrumentation Amplifier

The low-input-resistance problem can be solved by using voltage followers to buffer the two input terminals. We can achieve gain without compromising the high input resistance simply by using followers with gain rather than unity-gain followers.

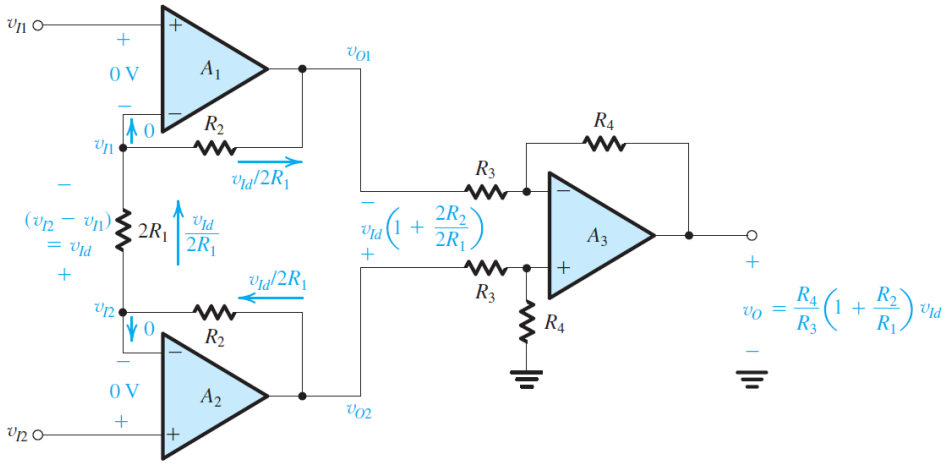
$$\boldsymbol{v_o = \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right)v_{id}}$$



Problems of this circuit:

- v_{Icm} is amplified in the first stage. The op could saturate in the second stage.
- The two amplifier channels in the first stage have to be perfectly matched, otherwise a spurious signal may appear between their two outputs.
- To vary A_d two resistors have to be varied simultaneously and be perfectly matched

Solution. The gain can be varied by changing only one resistor $2R_1$



2.5. Frequency Response of Amplifiers

2.5.1. Sinusoidal circuits review

Valore efficace sinusoidale: $A = \frac{A_m}{\sqrt{2}}$

$\boldsymbol{A_m \sin(\omega t + \alpha) = \sqrt{2} A \sin(\omega t + \alpha)}$

$\cos(x) = \sin(x + \frac{\pi}{2})$

Forma polare: $\overline{A} = Ae^{j\alpha}$

Forma cartesiana: $\overline{A} = Acos(\alpha) + jAsin(\alpha)$

$A = |\overline{A}| = \sqrt{Re^2 + Im^2}$

$$\alpha = \begin{cases} arctan\frac{Im}{Re} & se\ Re > 0 \\ +\frac{\pi}{2} & se\ Re = 0, Im > 0 \\ -\frac{\pi}{2} & se\ Re = 0, Im < 0 \\ arctan\frac{Im}{Re} \pm \pi & Re < 0 \end{cases}$$

Sfasamento: $\boldsymbol{\theta = \alpha - \beta}$

$\theta > 0$ α è $in\ anticipo$

$\theta < 0$ α è $in\ ritardo$

$\theta = 0$ $in\ fase$

$\theta = \pm\pi$ $opposizione\ di\ fase$

$\theta = +\pi/2$ α è $in\ quadratura\ in\ anticipo$

$\theta = -\pi/2$ α è $in\ quadratura\ in\ ritardo$

Inductor:

$v(t) = L * i'(t) = \omega L \angle 90°$

$\boldsymbol{\overline{Z} = jX_L = j\omega L = sL}$

$\theta = 90°$

Conductor:

$i(t) = C * u'(t)$

$\boldsymbol{\overline{Z} = jX_C = -j\frac{1}{\omega C} = \frac{1}{sC}}$

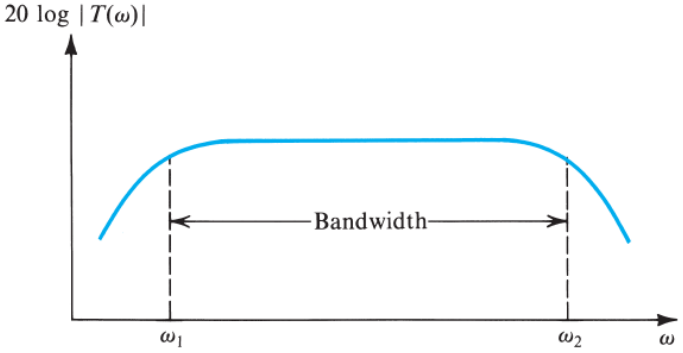
$\theta = -90°$

2.5.2. Frequency Response

Input signal to an amplifier can always be expressed as the sum of sinusoidal signals, so we study its response at different frequencies.

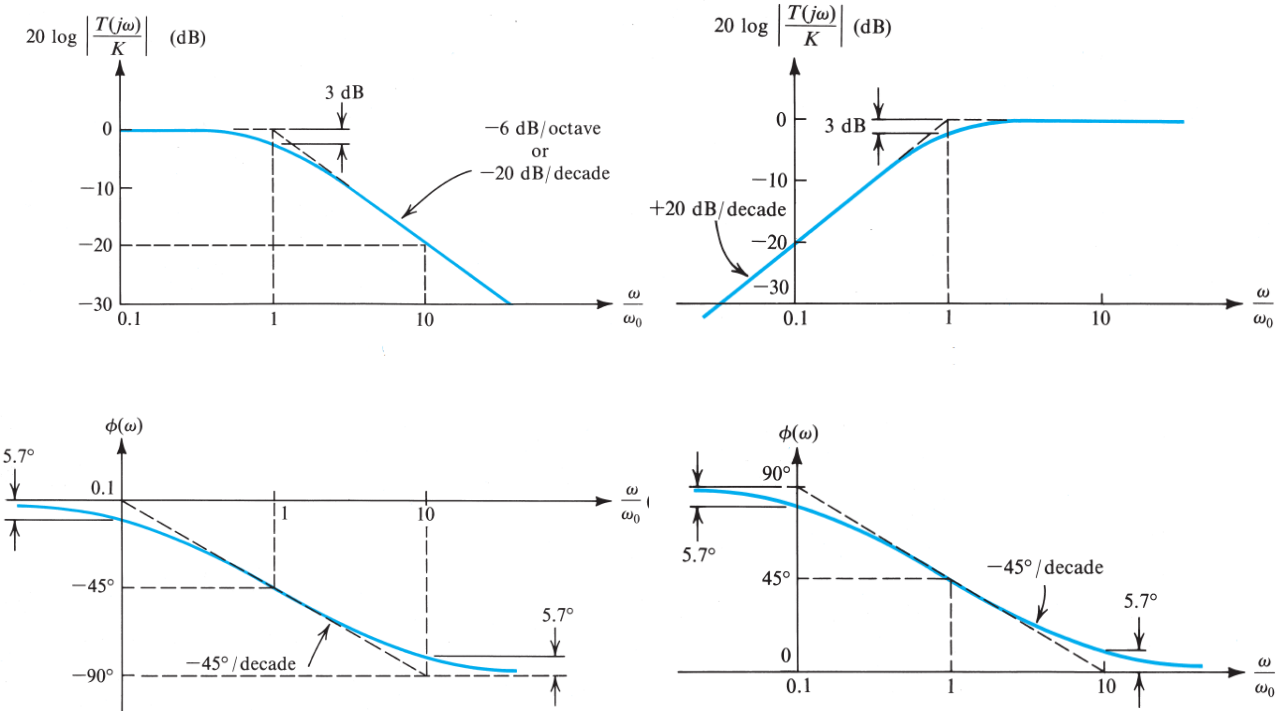
Whenever a sine-wave signal is applied to a linear circuit, the resulting output is sinusoidal with the same frequency as the input.

Amplifier bandwidth: band of frequencies over which the gain of the amplifier is almost constant, to within a certain number of decibels (usually 3 dB).



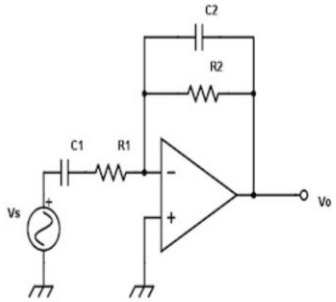
Single-Time-Constant Networks: composed of 1 reactive component. Can be classified into two categories, low pass (LP) and high pass (HP).

	Low-Pass (LP)	High-Pass (HP)
Transfer Function $T(s)$	$\frac{K}{1+(s/\omega_0)}$	$\frac{Ks}{s+\omega_0}$
Transfer Function (for physical frequencies) $T(j\omega)$	$\frac{K}{1+j(\omega/\omega_0)}$	$\frac{K}{1-j(\omega_0/\omega)}$
Magnitude Response $\lvert T(j\omega)\rvert$	$\frac{\lvert K\rvert}{\sqrt{1+(\omega/\omega_0)^2}}$	$\frac{\lvert K\rvert}{\sqrt{1+(\omega_0/\omega)^2}}$
Phase Response $\angle T(j\omega)$	$-\tan^{-1}(\omega/\omega_0)$	$\tan^{-1}(\omega_0/\omega)$
Transmission at $\omega = 0$ (dc)	K	0
Transmission at $\omega = \infty$	0	K
3-dB Frequency	$\omega_0 = 1/\tau$; $\tau \equiv$ time constant $\tau = CR$ or L/R	



To determinate $\tau = RC \; or \; L/R$ where R = equivalent resistance at the two terminals of C(or L) with generators turned off.

All band pass filter:



$$-\frac{C_1 R_2}{(1+sC_1R_1)(1+sC_2R_2)}$$

2.5.3. Transfer functions

Evans: $\boldsymbol{W(s) = \frac{b(s)}{a(s)} = K_E \frac{\prod_{k=1}^{m}(s-z_k)}{\prod_{k=1}^{n}(s-p_k)}}$

Bode: $W(s) = \frac{K_B}{s^l} \frac{\prod_k (1+sT_k)^{v_k}}{\prod_k (1+s\overline{T}_k)^{\overline{v}_k}}$

From Evans to bode: $\boldsymbol{s - z = -z(1 + s\tau)}$ $con\ \tau = -1/z$

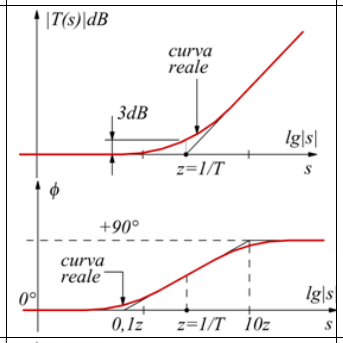
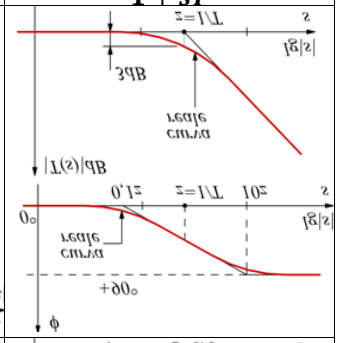
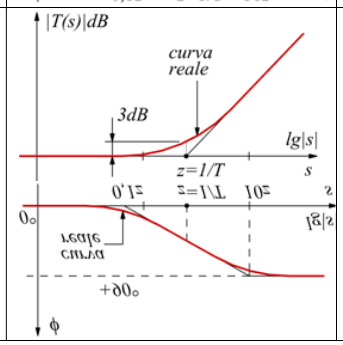
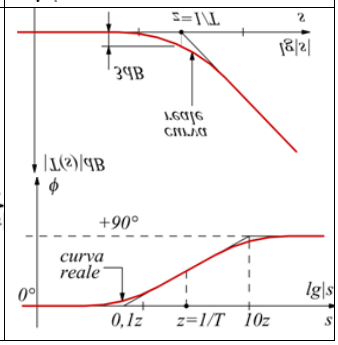
$$3dB = \sqrt{2}$$
$$6dB = 2$$
$$20dB = 10$$

$$|W(j\omega)|_{dB} = \left|\frac{K_B}{(j\omega)^l}\right|_{dB} + \sum_k v_k |1 + j\omega T_k|_{dB} - \sum_k \overline{v}_k |1 + j\omega \overline{T}_k|_{dB}$$

Come fare:

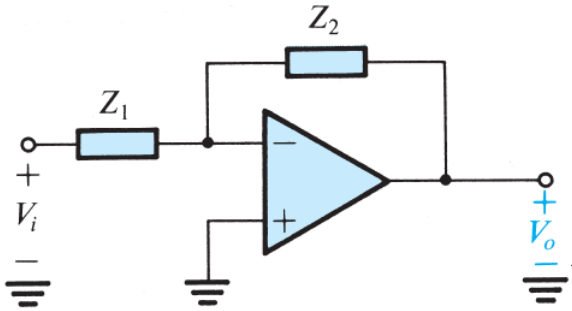
- Riduci a $W(s) = \frac{K_B}{s^l} \frac{\prod_k (1+sT_k)^{v_k}}{\prod_k (1+s\overline{T}_k)^{\overline{v}_k}}$
- Disegna punti di spezzamento: $\left|\frac{1}{T_k}\right|, \left|\frac{1}{\overline{T}_k}\right|, \boldsymbol{\omega_{nk}, \overline{\omega}_{nk}}$
- Modulo:
  - Disegna $\frac{K_B}{s^l}$: **Retta** con pendenza: $\boldsymbol{-20l}$ dB/dec e **intersezione** asse y: $\boldsymbol{20log|K_B|}$
  - Ad ogni punto di spezzamento la pendenza varia di: $v_k: +20, \overline{v}_k: -20$
- Fase:
  - Disegna $\frac{K_B}{s^l}$: Retta orizzontale: $\begin{cases} -l\frac{\pi}{2}, & K_B > 0 \\ -l\frac{\pi}{2} - \pi, & K_B < 0 \end{cases}$
  - Ad ogni punto di spezzamento la fase varia di: $v_k: \begin{cases} +\frac{\pi}{2}\ se\ T > 0 \\ -\frac{\pi}{2}\ se\ T < 0 \end{cases}, \overline{v}_k: \begin{cases} -\frac{\pi}{2}\ se\ \overline{T} > 0 \\ +\frac{\pi}{2}\ se\ \overline{T} < 0 \end{cases}$,

    Contando che inizia una decade prima e finisce una decade dopo

	$\boldsymbol{1 + sT}$	$\boldsymbol{\frac{1}{1 + sT}}$
T>0		
T<0		

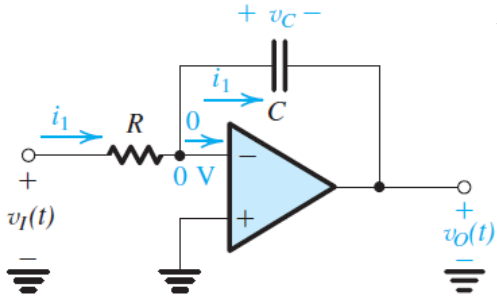
2.6. Integrators and Differentiators

Inverting Configuration with General Impedances:



$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)}$$

Inverting Integrator (low pass filter): -20dB



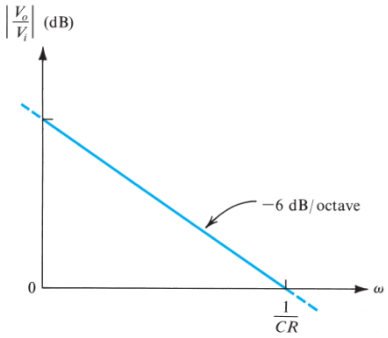
$$\boldsymbol{v_o(t) = -\frac{1}{CR}\int_0^t v_i(t)dt - V_C}$$

$$\boldsymbol{T(s) = \frac{V_o(s)}{V_i(s)} = -\frac{1}{sCR} = -\frac{1}{j\omega CR}}$$

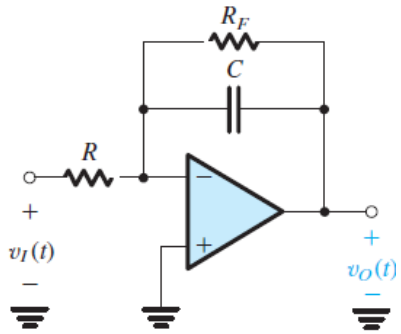
$$|T(s)| = \frac{1}{\omega CR}$$

$$\angle(T(s) = +90°$$

$$\omega_{int} = \frac{1}{\tau} = \frac{1}{CR}$$

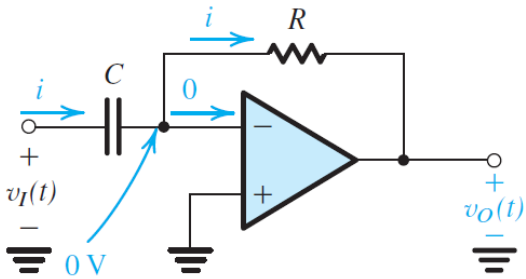


Problem: Any tiny dc component in the input signal will produce an infinite output.
Solution: connecting a large resistor $R_F//C$ that provides a DC feedback.



$$T(s) = -\frac{R_F/R}{1+sCR_F}$$

Differentiator (High pass filter): +20dB



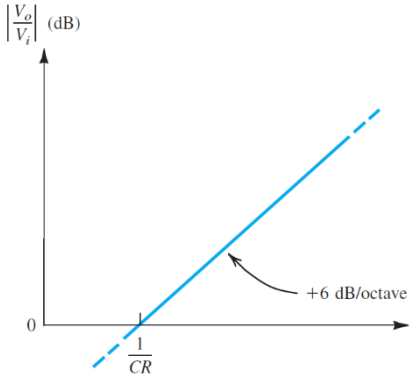
$$v_o(t) = -CR\frac{dv_i(t)}{dt}$$

$$T(s) = -sCR = -j\omega CR$$

$$|T(s)| = \omega CR$$

$$\angle(T(s) = -90°$$

$$\omega_L = \frac{1}{\tau} = \frac{1}{CR}$$



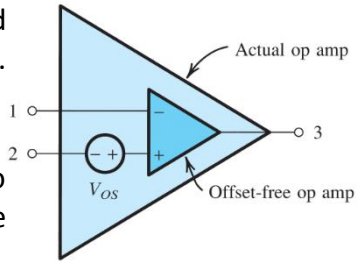
Problems: amplifies noise in high frequencies and is instable.
Solution: connect a **small resistor R_1** in series with C. $T(s) = \frac{-sR_2/R_1}{s+\frac{1}{CR_1}}$

2.7. Non-Ideal Op-Amp

2.7.1. DC Imperfections

The nonideal properties of op amps will limit the range of operation of the circuits.

DC Offset Voltage: if the two input terminals are tied together and connected to ground, despite $v_{Id} = 0$, $\boldsymbol{v_o \neq 0}$, and actually $v_o = \pm v_{sat}$.
It is like there is an input offset voltage V_{OS} usually $1 \div 5mV$



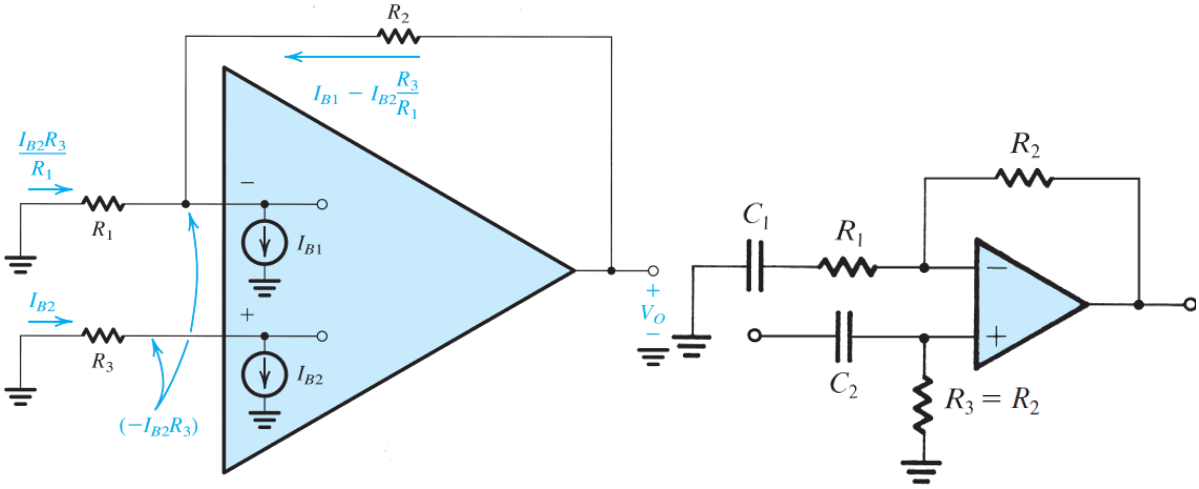
Solutions:

- Some op-amp are provided with two additional terminals to which a specified circuit can be connected to trim to zero the output dc voltage.
  But the problem remains of the variation (or drift) of V_{OS} with temperature.
- Adding a Capacitor C in series with R_1. But this will cause problem with low frequency input signals.

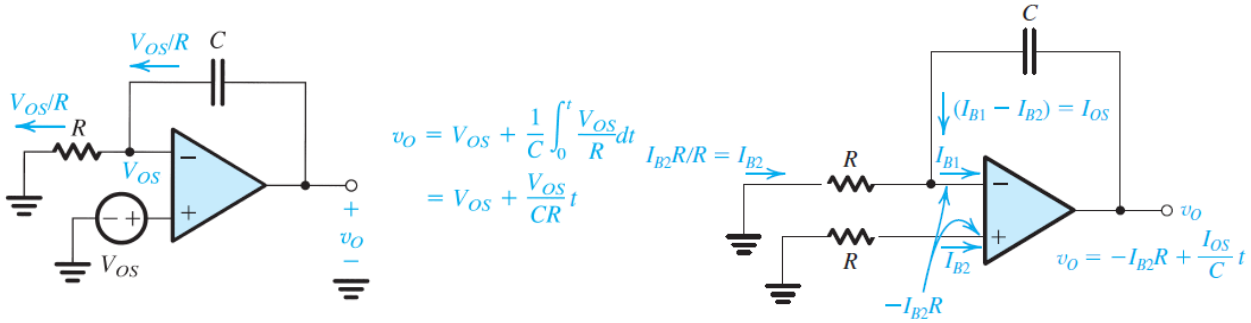
Input Bias and Offset Currents: input currents are not zero.

- **Input bias current:** $\boldsymbol{I_B = \frac{I_{B1}+I_{B2}}{2}}$ typical 100nA
- **Input Offset current:** $\boldsymbol{I_{OS} = |I_{B1} - I_{B2}|}$ typical 10nA

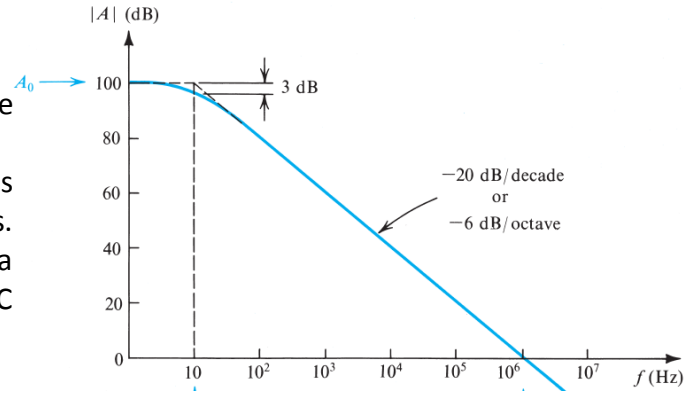
Solution: add resistor $R_3 = R_1 // R_2$, if the op-amp is AC coupled: $R_3 = R_2$



Effect of V_{OS} and I_{OS} on inverting Integrator: the op-amp saturates quickly.



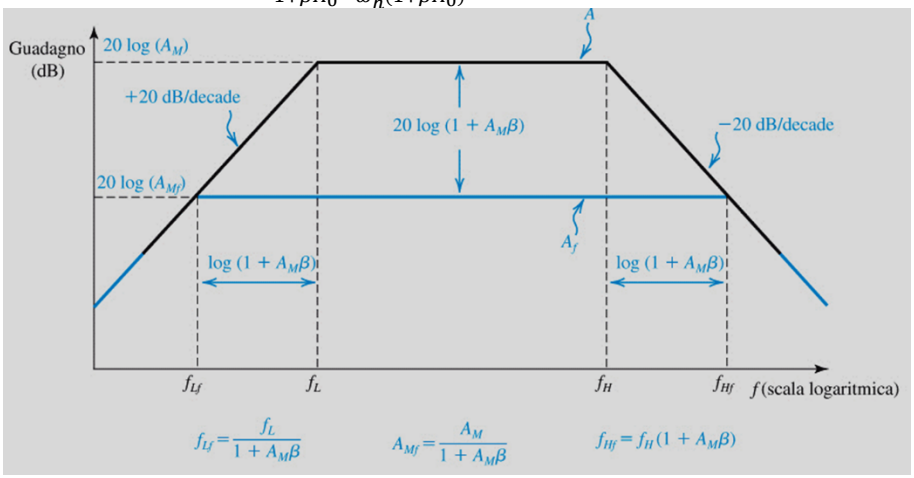
2.7.2. Effects on frequency response



The open-loop gain $\boldsymbol{A}$ **is not infinite**, its finite **and decrease** with frequency.
The uniform –20-dB/decade gain rolloff is typical of internally compensated op amps. These are units that have a network (usually a single capacitor) included within the same IC chip.

Without feedback: $A(s) = \frac{A_0}{1+s/\omega_b}$

With feedback: $A_f(s) = \frac{A(s)}{1+A(s)\beta} = \frac{\frac{A_0}{1+\beta A_0}}{\frac{1+\beta A_0}{1+\beta A_0}+\frac{s}{\omega_h(1+\beta A_0)}}$, A_0 decreases, ω_h increases



2.7.3. Large-Signal Operation

Output Voltage Saturation: an op amp that is operating from±15-V supplies will saturate when the output voltage reaches about ± 13

Output Current Limits: output current is limited to a specified maximum. Usually $\pm 20mA$

Slew Rate: $\boldsymbol{SR} = \left.\frac{\boldsymbol{dv_o}}{\boldsymbol{dt}}\right|_{\boldsymbol{max}}$ $[V/\mu s]$ maximum rate of change possible at the output.
If the input signal applied to an op-amp circuit is such that it demands an output response that is faster than the specified value of SR, the op amp will not comply. Rather, its output will change at the maximum possible rate.

Full-power bandwidth: $\boldsymbol{f_M} = \frac{\boldsymbol{SR}}{\boldsymbol{2\pi V_{Omax}}}$ frequency at which an output sinusoid with amplitude equal to the rated output voltage of the op amp begins to show distortion due to slew-rate limiting.

Esercizi Esame:

- Calcola vo/vi
- R_i : applying an input voltage v_i and measuring the input current i_i. $R_i = v_i/i_i$
- R_o: eliminating the input signal source and applying a voltage signal $v_x = 0??$ to the output of the amplifier. $R_o = v_x/i_x$. $i' = grande\ a\ piacere\ uscente$
- W(s) bode
    - $\frac{1}{sC}\ e\ sL$
    - …
- $\boldsymbol{v_o = A_d v_{id} + A_{cm} v_{icm} = \left(\frac{A_2 - A_1}{2}\right) v_{id} + (A_1 + A_2) v_{cm}}$
  $v_{Id} = v_2 - v_1 \;\; v_{Icm} = \frac{1}{2}(v_2 + v_1)$

$$\mathbf{CMRR|_{dB} = 20 \log \frac{|A_d|}{|A_{cm}|}}$$

3.Semiconductors

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3.1. The PN Junction

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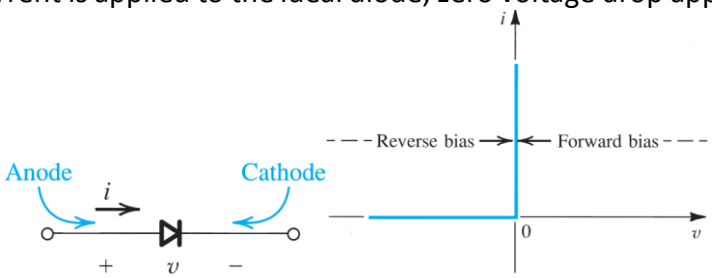
4. Diodes

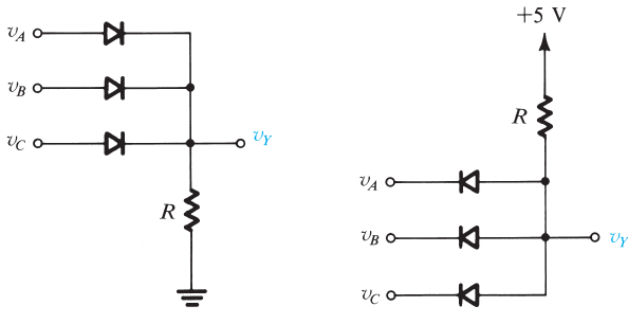
4.1. The Ideal Diode

Current–Voltage Characteristic:

- If a negative voltage is applied to the diode, no current flows and the diode behaves as an open circuit.
- If a positive current is applied to the ideal diode, zero voltage drop appears across the diode.



Logic gates with diodes: OR & AND



4.2. Terminal Characteristics of Junction Diodes

The forward-bias region $v > 0$:

$$i = I_S\left(e^{\frac{v}{V_T}} - 1\right) \cong I_S e^{\frac{v}{V_T}}$$

$$v = V_T \ln\frac{i}{I_S}$$

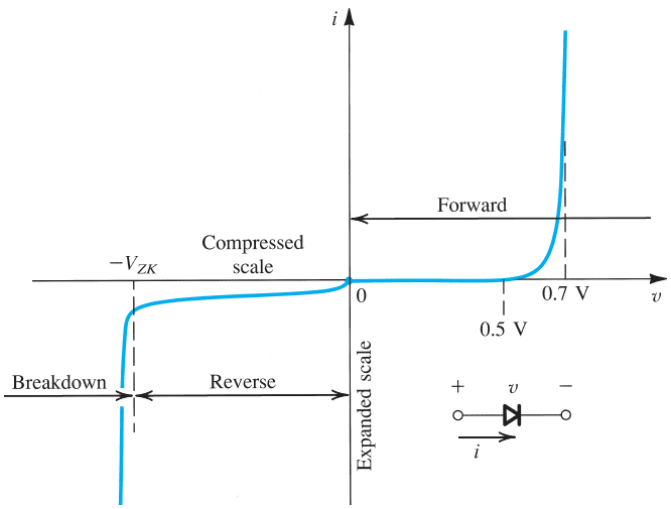
$$V_2 - V_1 = 2.3V_T \log\frac{I_2}{I_1}$$

v: voltage on the diode terminals
I_S: constant, reverse saturation current
$V_T = 25.3\ mV$: thermal voltage

$2.3V_T = 60\ mV$

The reverse-bias region $v < 0$: $i \cong -I_S$

The breakdown region $v < -V_{ZK}$:
The breakdown region is entered when the magnitude of the reverse voltage exceeds a threshold value that is specific to the particular diode, called the breakdown voltage.

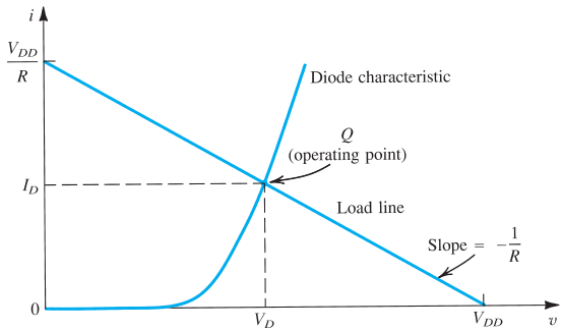


4.3. Models

4.3.1. Exponential

Is most accurate description of the diode operation in the forward region however, its the most difficult to use. $I_D = I_S e^{\frac{V_D}{V_T}}$ e $I_D = \frac{V_{DD} - V_D}{R}$

Graphical analysis:



Iterative analysis:

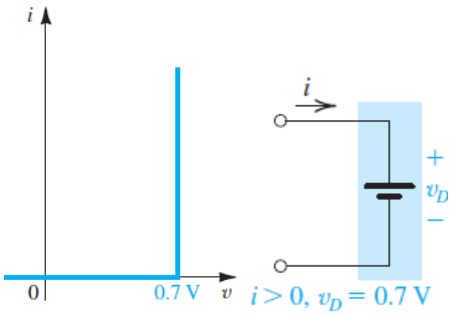
1° Iteration:

- $I_2 = I_D = \frac{V_{DD} - V_D}{R}$
- $V_2 = 2.3V_T \log \frac{I_2}{I_1} + V_1$ where $2.3V_T = 60mA, I_1 = desired, V_1 = V_D$

2° Iteration:

- $I_2' = I_D = \frac{V_{DD} - V_2}{R}$
- $V_2' = 2.3V_T \log \frac{I_2'}{I_2} + V_2$

4.3.2. Constant-Voltage-Drop Model



$V_D = 0.7\ V$

Potenza $P = V_D * i$

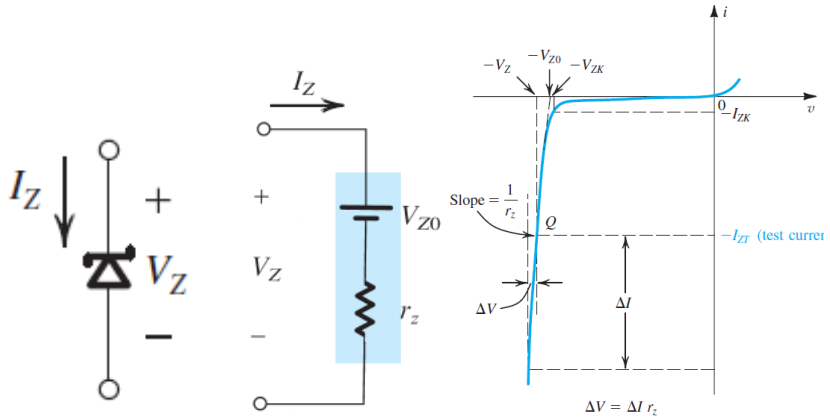
4.3.3. Ideal Model

In applications that involve voltages much greater than the diode voltage drop (0.6 V–0.8 V), we may neglect the diode voltage drop. The greatest utility of the ideal-diode model is in determining which diodes are on and which are off in a multidiode circuit.

4.3.4. The Small-Signal Model: $r_d = V_T/i$

4.4. Zener diodes

Special diodes are manufactured to operate specifically in the breakdown region.
For currents greater than the knee current IZK the i–v characteristic is almost a straight line.



$$V_Z = V_{Z0} + r_Z I_Z$$

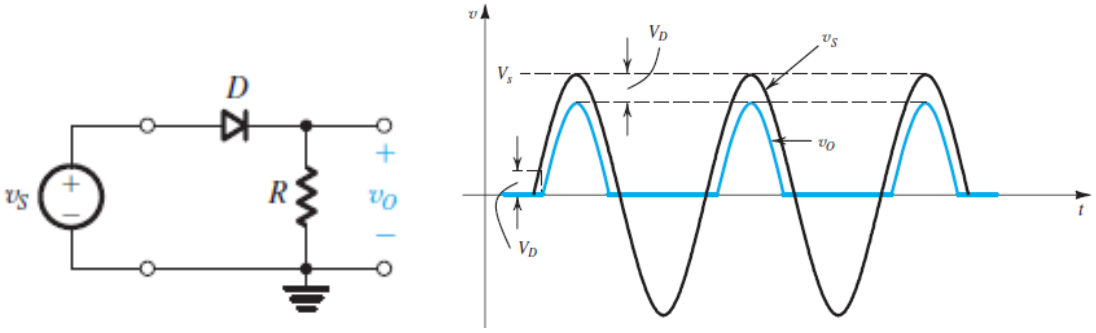
4.5. Rectifier Circuits

In selecting diodes for rectifier design, two important parameters must be specified:

- The **current-handling capability** required of the diode, determined by the largest current the diode is expected to conduct
- The **peak inverse voltage (PIV):** the diode must be able to withstand without breakdown, determined by the largest reverse voltage that is expected to appear across the diode.

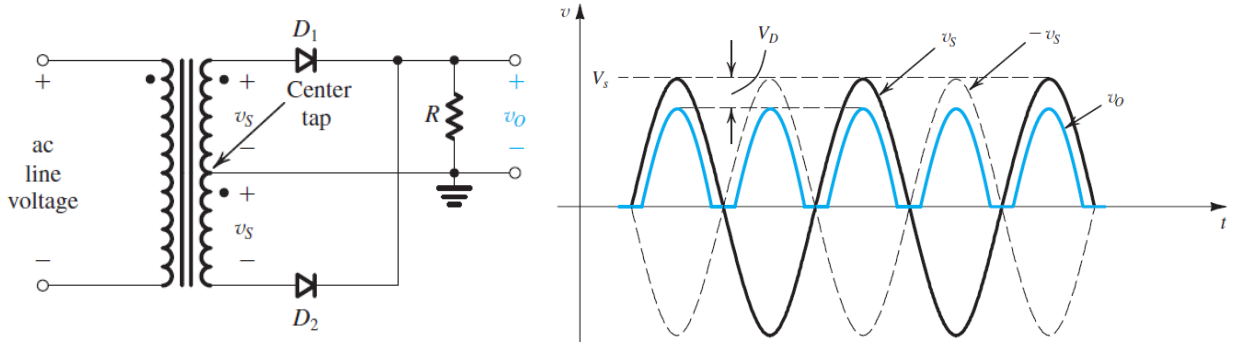
The Half-Wave Rectifier

$$v_O = 0, \qquad v_S < V_D$$
$$v_O = v_S - V_D, \qquad v_S \geq V_D \qquad PIV = V_s$$

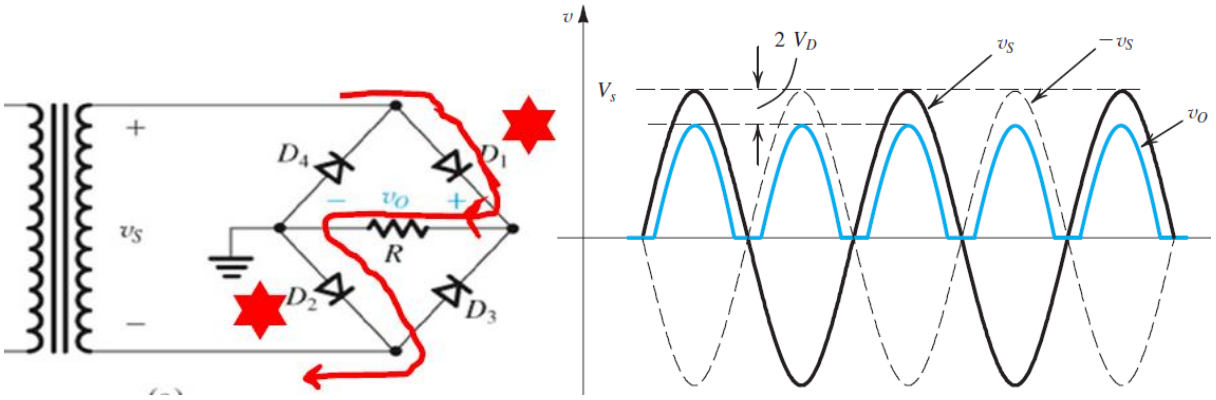


The Full-Wave Rectifier

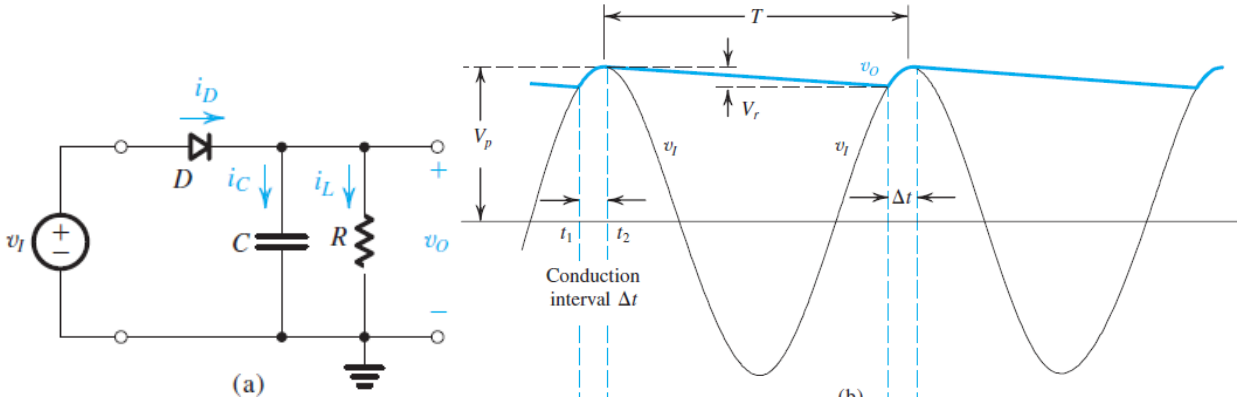
Inverts the negative halves of the sine wave. $PIV = 2V_s - V_D$



The Bridge Rectifier (Wheatstone): does not require a center-tapped transformer. $PIV = V_s - V_D$



The Peak Rectifier: A simple way to reduce the variation of the output voltage is to place a capacitor across the load resistor.



$I_L = (V_p - V_{on})/R$

When diode is off: $v_o = V_p e^{-T/RC}$

Ripple voltage: $V_r = (V_p - V_{on})\frac{T}{RC} = \frac{V_p}{2fCR}$

$V_p - V_r = V_p \cos(\omega \Delta t)$

Angle $\theta = \omega \Delta t = \sqrt{2V_r/V_p}$

Average diode current: $i_{Dav} = I_L\left(1 + \pi\sqrt{2V_p/V_r}\right)$

Peak value: $i_{Dmax} = I_L\left(1 + 2\pi\sqrt{2V_p/V_r}\right)$

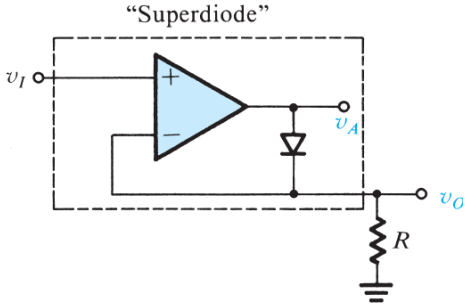
Corrente di picco: $I_P = I_L \frac{2T}{\Delta t}$ (una semionda)

Corrente di spunto: $I_{SC} = \omega C V_P$ (una semionda)

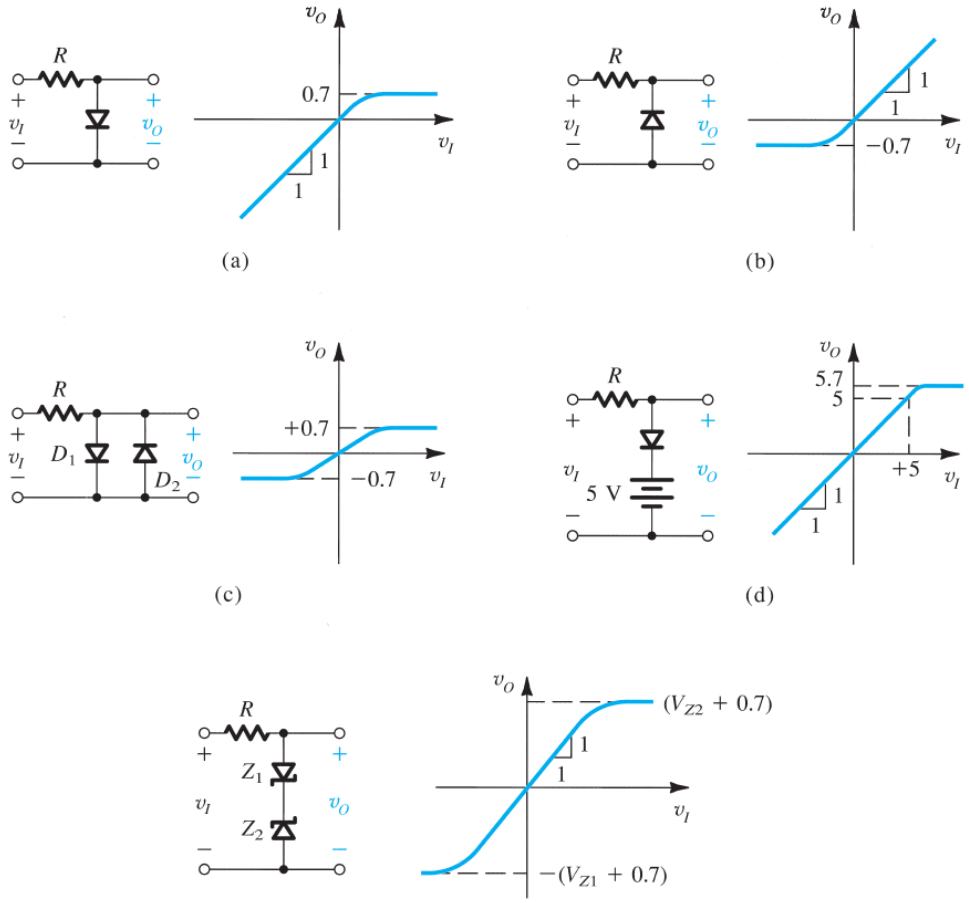
A doppia semionda semplicemente T-->T/2

Dissipazione diodo: $P_D = V_{on} * I_L$

Precision Half-Wave Rectifier—The Superdiode: Used when the signal to rectify is smaller than V_{on}



4.6. Limiting and Clamping Circuits



Esercizi Esame:

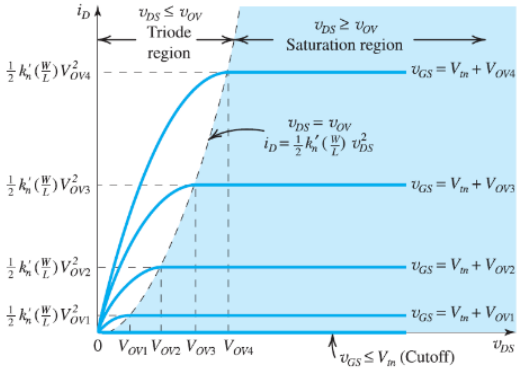
- Se considerato ON: $I_D > 0$
- Se considerate OFF: $V_D < V_\gamma$

Come si risolve un circuito a diodi

a) si formula un'ipotesi sullo stato dei diodi
b) si trovano tensioni e correnti sulla base dell'ipotesi formulata
c) si verifica che la soluzione sia coerente con l'ipotesi formulata:
   - nel caso si sia ipotizzato il diodo in diretta
     - VA > 0 o VA > 0.7 V secondo il modello usato
     - corrente positiva entrante nel diodo nel verso della freccia
   - nel caso si sia ipotizzato il diodo in inversa (OFF)
     - VA < 0 V
     - corrente nel diodo nulla

5. MOS Field-Effect Transistors (MOSFETs)

5.1. Basics

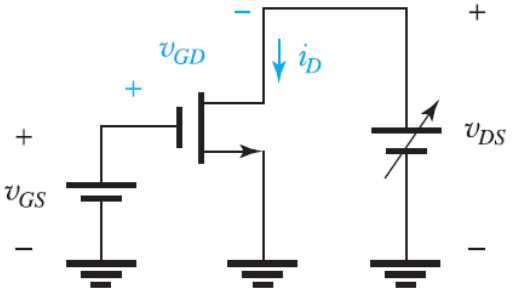


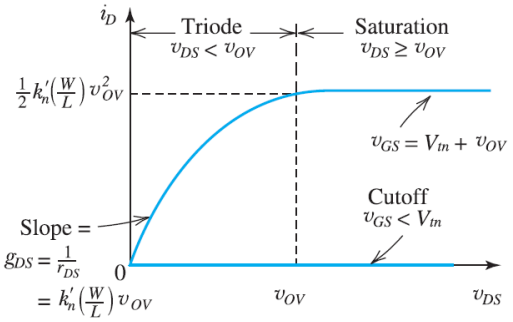
Proprieties:

- $i_G = 0$
- Threshold voltage $v_t = 0.3 \div 1.0V$
- Overdrive voltage $|v_{OV}| = |v_{GS}| - |V_t|$
- Process transconductance $k_n' = \mu_n C_{ox}$
- Transconductance parameter $k_n = (\mu_n C_{ox})\left(\frac{W}{L}\right)$ $\left[\frac{A}{V^2}\right]$

n-mos:

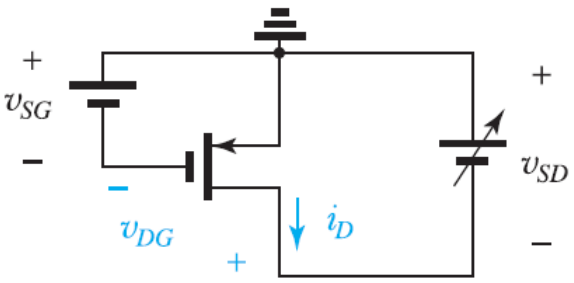
- $v_{GS} < V_{tn}$: OFF $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$ ON:
  - **Triode** Region: $\boldsymbol{v_{GD} > V_{tn}}$ or $v_{DS} < v_{OV}$
    - $i_D = k_n\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$
    - Conductance $g_{DS} = k_n(v_{GS} - V_t)$
    - Resistance $r_{DS} = \frac{1}{g_{DS}} \cong \frac{V_{DS}}{I_D}$ For $v_{GS} \le V_t \rightarrow r_{DS} = \infty$
  - **Saturation** Region: $\boldsymbol{v_{GD} \le V_{tn}}$ or $v_{DS} \ge v_{OV}$
    - $i_D = \frac{1}{2}k_n(v_{GS} - V_{tn})^2(1 + \lambda v_{DS})$

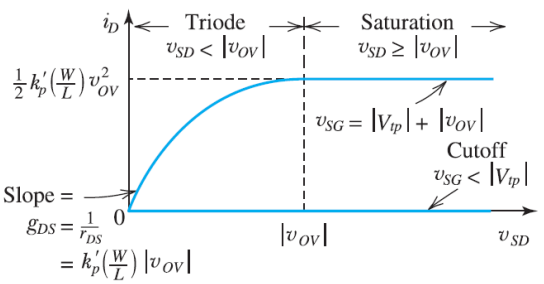




p-mos:

- $v_{SG} < |V_{tp}|$ OFF: $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$ ON:
  - **Triode** Region: $v_{DG} > |V_{tp}|$ or $v_{SD} < |v_{OV}|$
    - $i_D = k_n\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$
  - **Saturation** Region: $\boldsymbol{v_{DG} \le |V_{tp}|}$ or $v_{SD} \ge |v_{OV}|$
    - $i_D = \frac{1}{2}k_n(v_{SG} - |V_{tp}|)^2(1 + |\lambda|v_{SD})$





Esercizi:

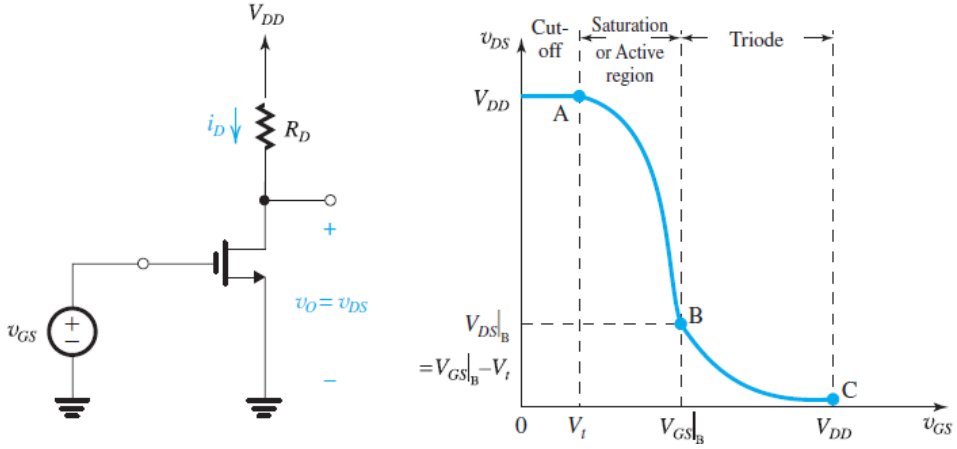
- Look if its ON or OFF
- Look if is Triode or Saturation. Se non lo so: assumo saturazione, poi verifico che sia corretto.

5.2. Transistor Amplifiers

MOSFET is basically a transconductance amplifier: during saturation v_{GS} controls $i_D = \frac{1}{2}k_n(v_{GS} - V_{tn})^2$

Obtaining a Voltage Amplifier: $v_o = v_{DS} = V_{DD} - i_D R_D$

Voltage-Transfer Characteristic (VTC): Plot of the output voltage versus the input voltage.



Obtaining Linear Amplification by Biasing the Transistor

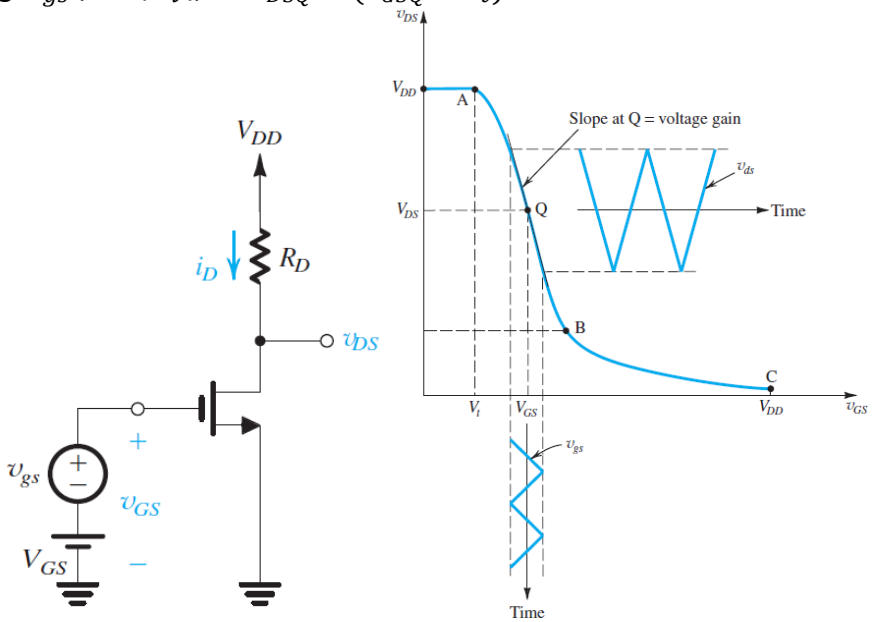
- A dc voltage V_{GS} is selected to obtain operation at a point Q on the segment AB of the VTC. Point Q is known as the bias point or the **dc operating point**.
- The signal to amplify $v_{gs}(t)$, is superimposed on the bias voltage V_{GS}. $v_{GS}(t) = V_{GS} + v_{gs}(t)$.

If v_{gs} is small enough to restrict the excursion of the instantaneous operating point to a short, almost-linear segment of the VTC around the bias point Q.

Voltage gain: $\boldsymbol{A_v = -k_n(V_{GS} - V_t)R_d = -\frac{I_D R_D}{V_{OV}/2} = -\frac{V_{DD} - V_{DS}}{V_{OV}/2}}$

Maximum voltage gain: $|A_{vMax}| = \frac{V_{DD} - V_{DS}|_B}{V_{OV}|_B/2} = \frac{V_{DD} - V_{OV}|_B}{V_{OV}|_B/2}$ is on point B

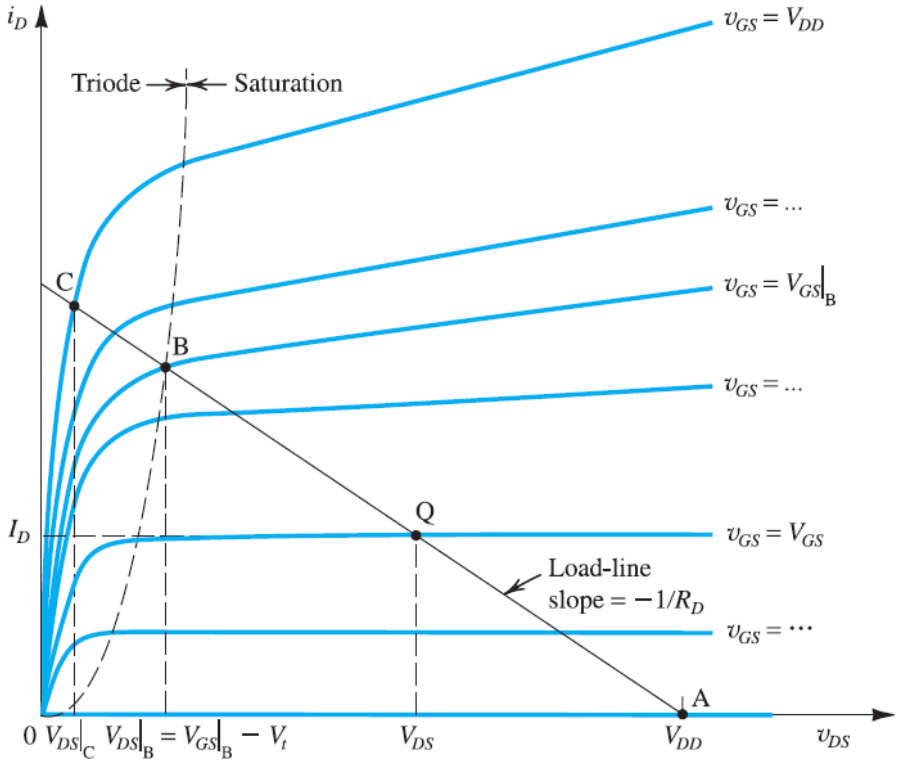
To avoid clipping: $v_{gs}(1 + |A_v|) < V_{DSQ} - (V_{GSQ} - V_t)$



Determining the VTC by Graphical Analysis:

Load line: straight line that represents the load resistance R_D.

- Point A: the transistor is a open switch
- Point C: the transistor is a closed switch



5.3. Small-Signal Operation and Models

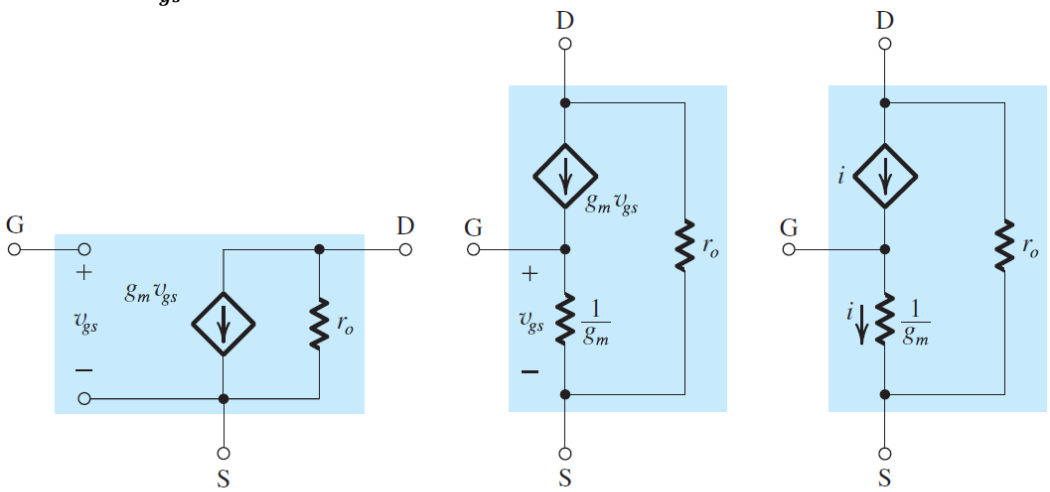
In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent-circuit model. The rest of the circuit remains unchanged except that ideal constant dc voltage sources are replaced by short circuits. Ideal constant dc current source can be replaced by an open circuit.

Small-signal condition: $v_{gs} \ll 2(V_{GS} - V_t)$ To reduce the nonlinear distortion

MOSFET transconductance: $g_m = \frac{i_d}{v_{gs}} = k_n(V_{GS} - V_t) = \sqrt{2k'_n}\sqrt{W/L}\sqrt{I_D} = \frac{2I_D}{V_{GS}-V_t}$

Output resistance: $r_o = \frac{|V_A|}{I_D}$ $[10k \div 1M]$ where $V_A = \frac{1}{\lambda}$, if ideal $\rightarrow r_o = \infty$

Voltage gain: $A_v = \frac{v_{ds}}{v_{gs}} = -g_m(R_D||r_o)$



Hybrid-π model T models

Solution of a problem for amplification:

- Calculate the DC point: i_D, v_{DS}
  - Eliminate any non-DC input signals
  - Capacitors → Open circuits
  - Inductors → Short
- Calculate the small signal parameters: gm, ro
- Only in mos where appears current o voltage variations (signals):
  - Substitute the MOS with the small signal model:
    - If a resistance is connected in the source lead, the T model is preferred.
  - Voltage generators become short (except Vi)
  - Current generators become open circuits
  - Capacitors → shorts
  - Inductors → open circuits
- Calculate A_v, R_i, R_o, …
  - R_i: applying an input voltage v_i and calculate the input current i_i. $R_i = v_i/i_i$
  - R_o: eliminating the input signal source and load R_L, apply a voltage signal v_x to the output of the amplifier. $R'_o = v_x/i_x$. If without R_D: $R_o = R'_o//R_D$

5.4. Basic configurations

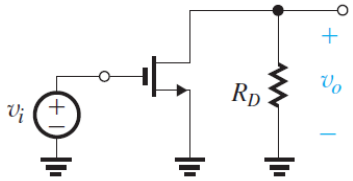
Three basic configurations for connecting a MOSFET as an amplifier, connecting one of the device terminals to ground.

We not include r_o in the initial analysis. At the end of the section we will offer a number of comments about when to include r_o.

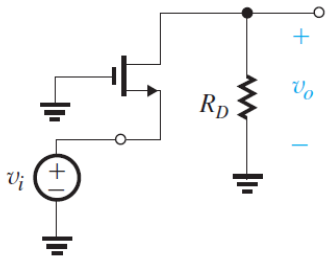
Considering r_o:

- Common Source: $R_D \rightarrow R_D // r_o$
- Common Drain: $R_L \rightarrow R_L // r_o$

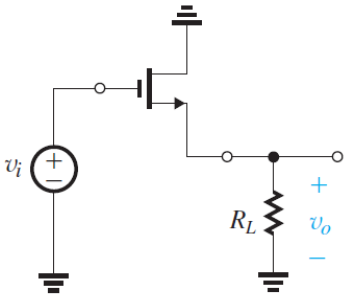
Usually we put a capacitor between the terminal and ground.



(a) Common Source (CS)

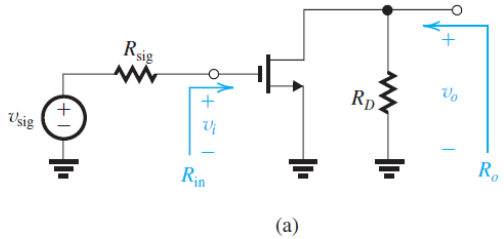


(b) Common Gate (CG)

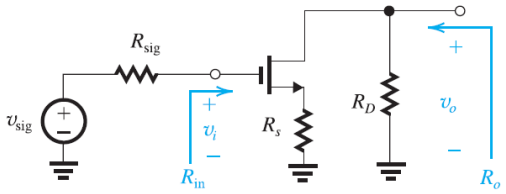


(c) Common Drain (CD) or Source Follower

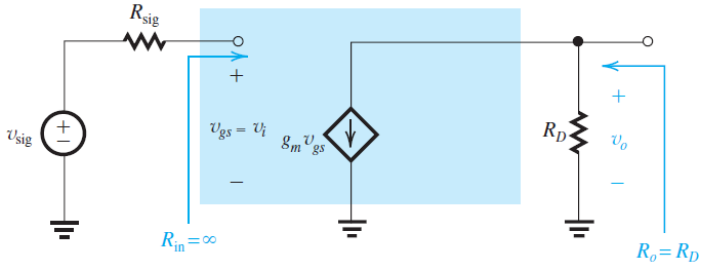
Common Source:

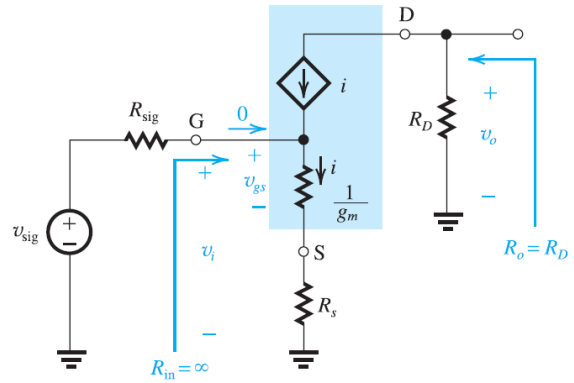


(a)

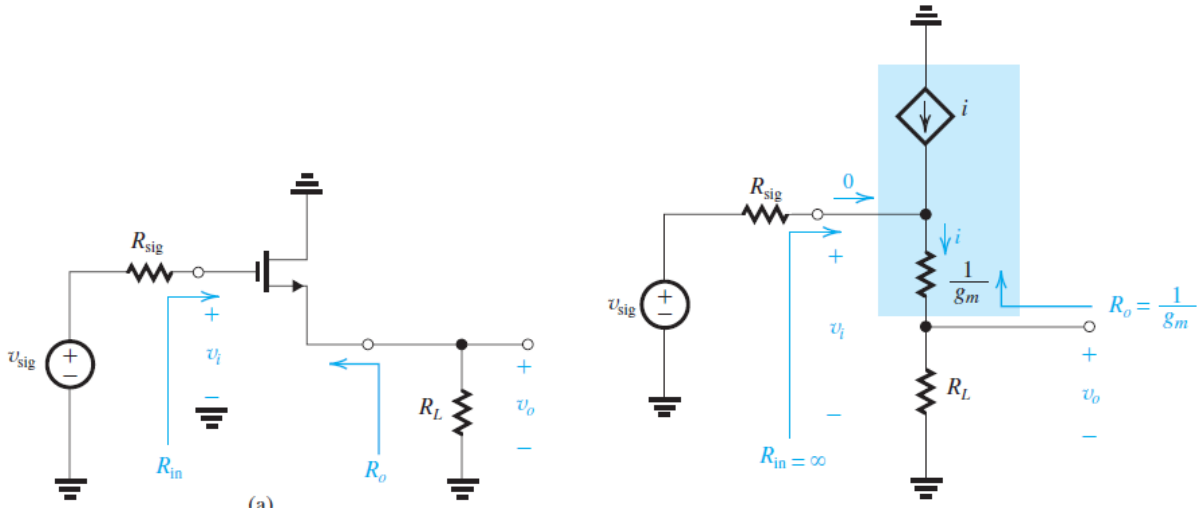


(a)

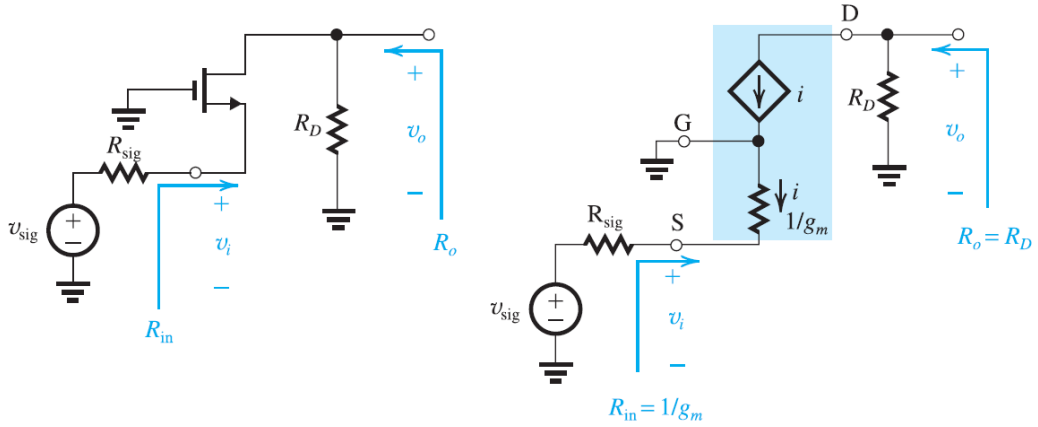




Common Drain (source follower):

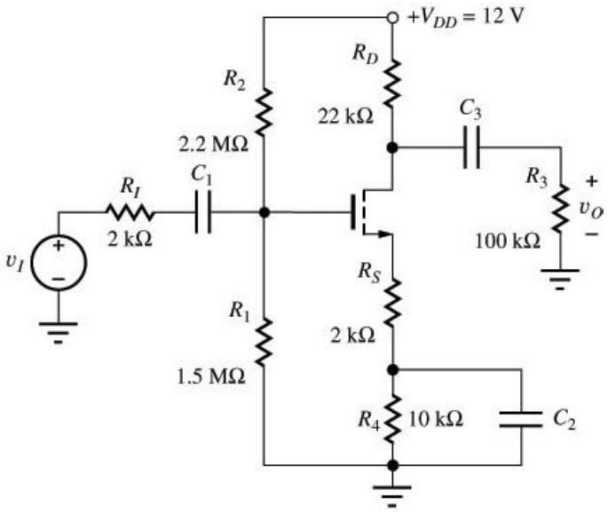


Common Gate:



Amplifier type	R_{in}	A_{vo}	R_o	A_v	G_v
Common source (Fig. 7.35)	∞	$-g_m R_D$	R_D	$-g_m(R_D \parallel R_L)$	$-g_m(R_D \parallel R_L)$
Common source with R_s (Fig. 7.37)	∞	$-\frac{g_m R_D}{1+g_m R_s}$	R_D	$\frac{-g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\frac{R_D \parallel R_L}{1/g_m + R_s}$	$-\frac{g_m(R_D \parallel R_L)}{1+g_m R_s}$ $-\frac{R_D \parallel R_L}{1/g_m + R_s}$
Common gate (Fig. 7.39)	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \parallel R_L)$	$\frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$
Source follower (Fig. 7.42)	∞	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$

Source:



$R_G = R_1//R_2$; $R_L = R_D//R_3$;

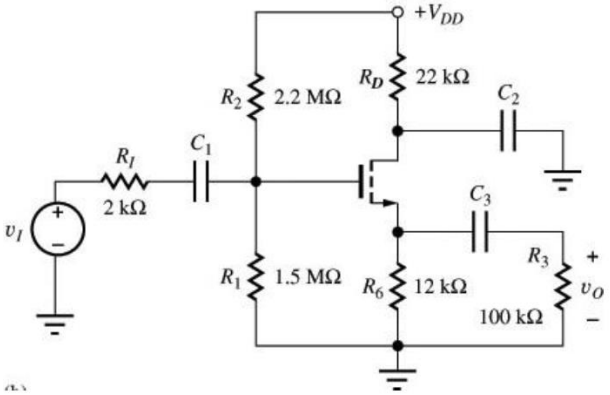
$$A_V = -\frac{g_m R_L}{1 + g_m R_S}\frac{R_G}{R_I + R_G}$$

$R_{IN}=R_G$

$R_{OUT}=r_o\,(1+g_mR_S)//R_D$

condizione di piccolo segnale
$v_g < 0.2(V_{GS} - V_T)\,(1+g_mR_S)$

Drain:



$R_G = R_1//R_2$; $R_L = R_6//R_3$;

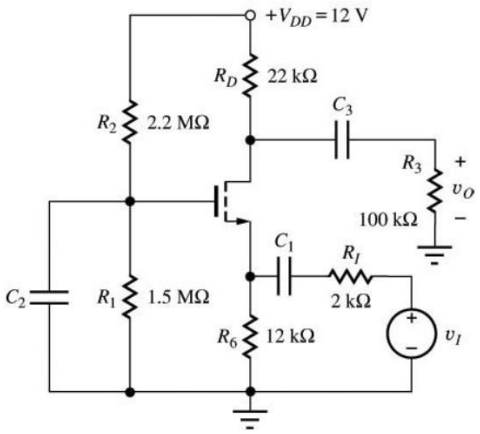
$$A_V = \frac{g_m R_L}{1 + g_m R_L}\frac{R_G}{R_I + R_G}$$

$R_{IN}=R_G$

$R_{OUT}= (1/g_m)//R_6 \cong 1/g_m$

condizione di piccolo segnale
$v_g < 0.2(V_{GS} - V_T)\,(1+g_mR_L)$

Gate:



$R_{TH} = R_6//R_I$; $R_L = R_6//R_3$;

$$A_V = \frac{g_m R_L}{1 + g_m R_{th}}\frac{R_6}{R_I + R_6}$$

$R_{IN}=1/g_m//R_6 \cong 1/g_m$

$R_{OUT}= r_o(1+g_mR_{th})$

condizione di piccolo segnale
$v_g < 0.2(V_{GS} - V_T)\,(1+g_mR_{TH})$

6. Integrated-Circuit Amplifiers

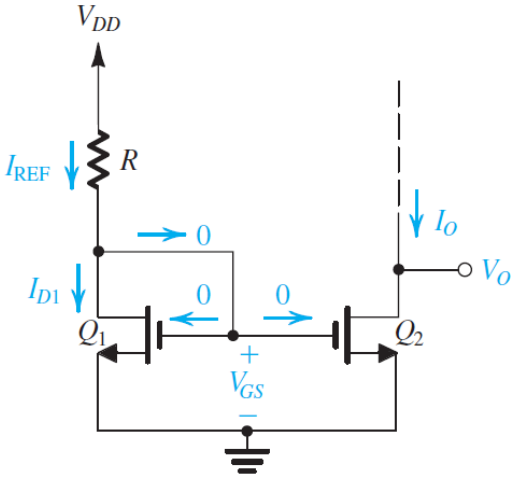
Important constraints and opportunities and the major feature:

- **Resistors:** large and even moderate-size resistors are to be avoided. Discourage the use of precise values. Use transistors in preference to resistors wherever possible. Collector and drain resistors in amplifiers are replaced with constant-current sources.
- **Capacitors**: it is impossible to fabricate large-valued capacitors, IC amplifiers are all direct coupled.
- **Power Supplies:** to avoid breaking down the thin oxide layers, power supplies are limited to 1 V.
- **Device Variety:** IC designer has the freedom to specify the device dimensions and to utilize device matching and arrays of devices having dimensions with specified ratios.
- **CMOS Technology:** vast majority of analog integrated circuits are designed using CMOS technology.

6.1. IC Biasing

Biasing in integrated-circuit design is based on the use of constant-current sources.
A constant dc current (called a **reference current**) is generated at one location and is then replicated at various other locations for biasing the various amplifier stages through a process known as **current steering**.

6.1.1. The Basic MOSFET Current Source



$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF}\left(1 + \lambda(V_O - V_{GS})\right)$$

Current Gain $\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}\left(1 + \lambda(V_O - V_{GS})\right)$

Current mirror: when identical transistors. $I_O = I_{REF}$

R in most cases would be outside the IC chip.

MOS Current-Steering Circuits

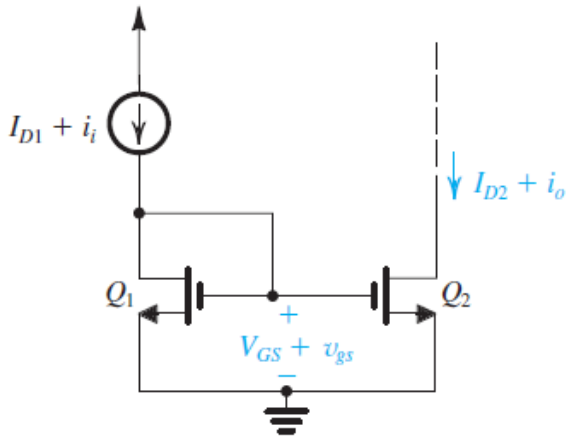
Once a constant current has been generated, it can be replicated to provide dc bias or load currents for the various amplifier stages in an IC. Current mirrors can be used to implement this current-steering function.

Current sink: pulls its current from a circuit.

Current source: pushes its current into a circuit.

6.1.2. Small-Signal Operation of Current Mirrors

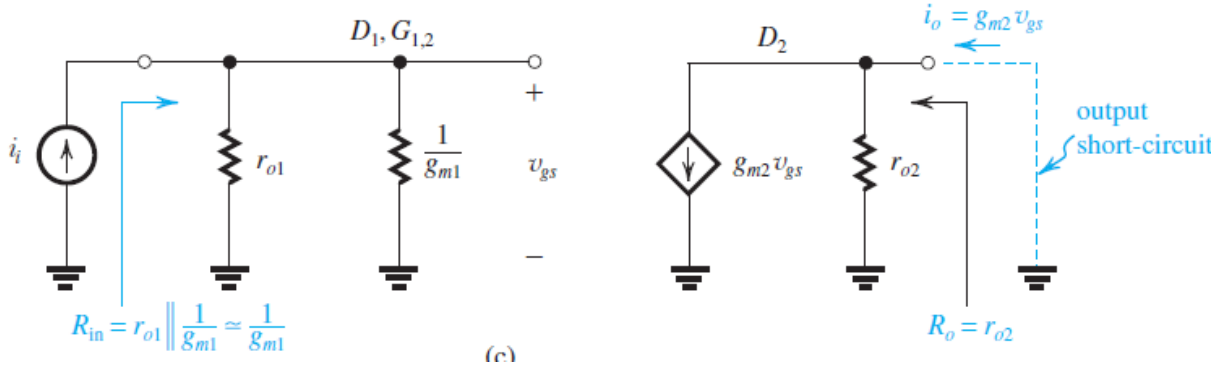
In addition to their use in biasing, current mirrors are sometimes employed as current amplifiers.



$$R_{in} = r_{o1} \| \frac{1}{g_{m1}} \cong \frac{1}{g_{m1}}$$

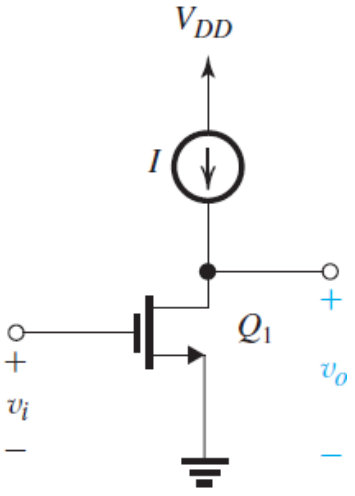
$$R_o = r_{o2}$$

$$A_{is} = \frac{g_{m2}}{g_{m1}} = \frac{(W/L)_2}{(W/L)_1}$$



6.2. The Basic Gain Cell

Is a common-source (CS) loaded with a constant-current source, replaced the resistances RD with constant-current sources.

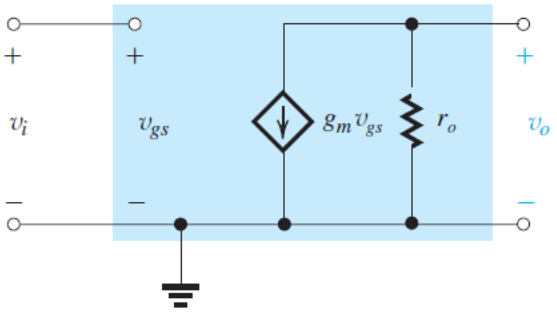


$$R_{in} = \infty$$

$$A_{vo} = -g_m r_o$$

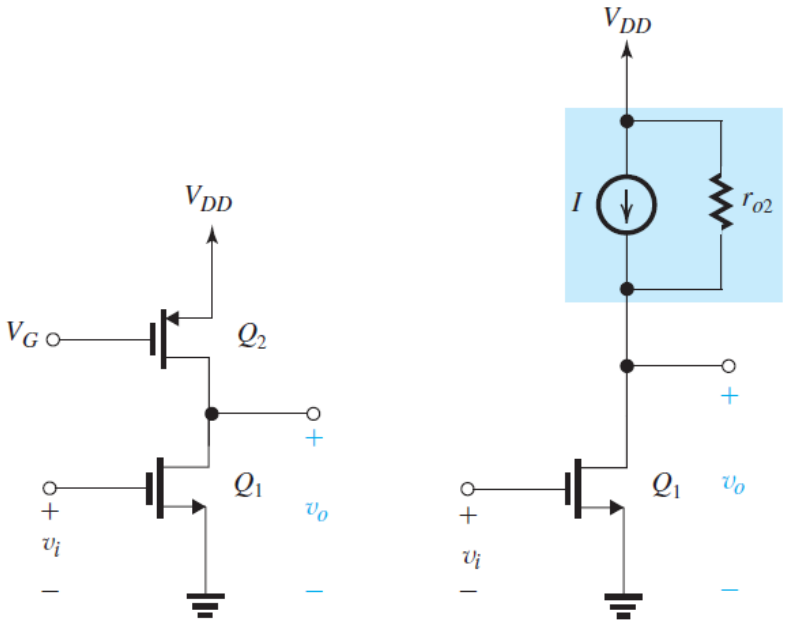
$$R_o = r_o$$

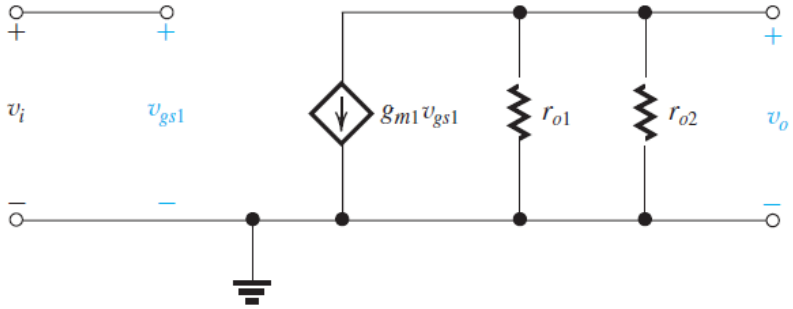
Intrinsic gain $A_0 = \frac{2V_A}{V_{OV}} = \frac{V_A' \sqrt{2(\mu_n C_{ox})(WL)}}{\sqrt{I_D}}$ *where* $V_A' = V_A/L$

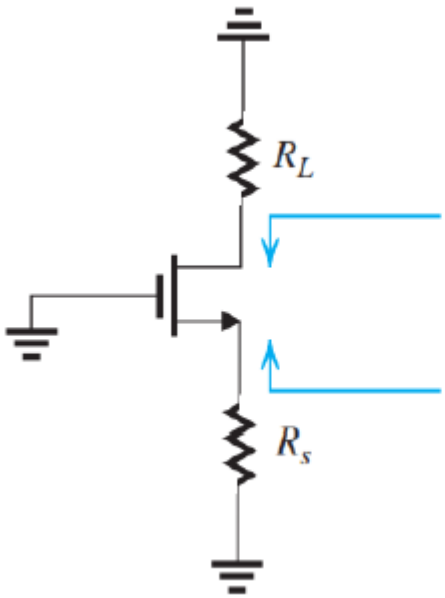


The current-source load of the CS amplifier can be implemented using a PMOS transistor biased in the saturation region to provide the required current.

$$A_v = \frac{v_o}{v_i} = -g_m(r_{o1} \| r_{o2})$$







$$R_{\text{out}} = r_o + R_s + g_m r_o R_s$$
$$\simeq r_o + (g_m r_o) R_s$$

$$R_{\text{in}} = \frac{r_o + R_L}{1 + g_m r_o}$$
$$\simeq \frac{1}{g_m} + \frac{R_L}{g_m r_o}$$

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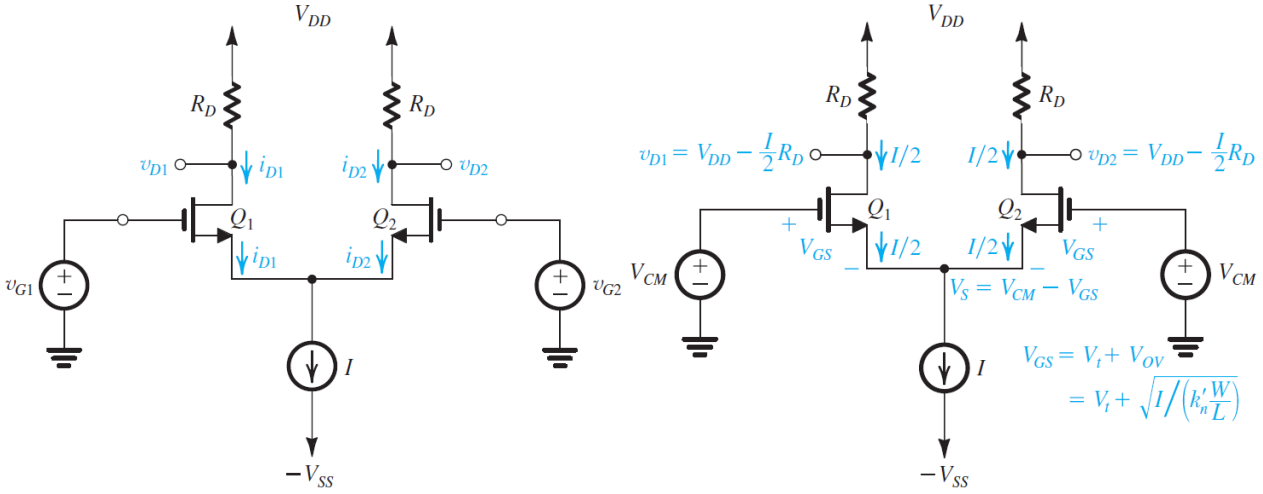
7.Differential Amplifiers

The differential-pair or differential-amplifier configuration is the most widely used building block in analog integrated-circuit design. Differential circuits are much less sensitive to noise.
The differential configuration **enables us to bias the amplifier and to couple amplifier stages together without the need for bypass and coupling capacitors.**

7.1. The MOS Differential Pair



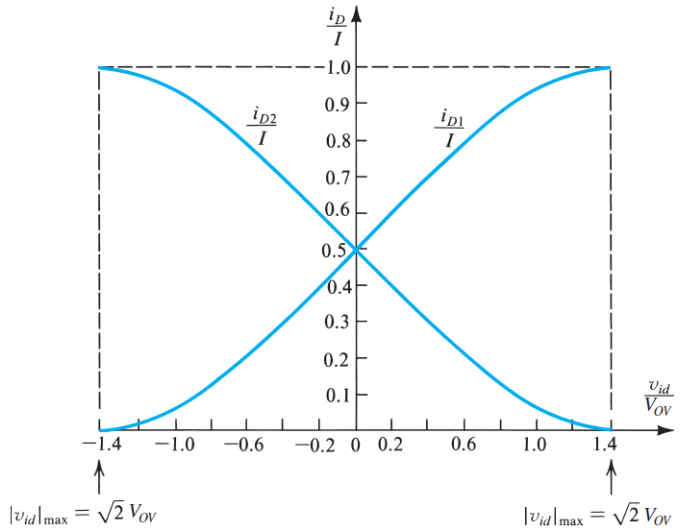
Common-Mode Input Voltage: $V_{CM} = v_{G1} = v_{G2}$

- $I_{D1} = I_{D2} = I/2$
- $V_{OV} = \sqrt{I/k_n}$

Input common-mode range: range of V_{CM} over which the differential pair operates properly.

- $V_{CMmax} = V_t + V_{DD} - \frac{I}{2}R_D$
- $V_{CMmin} = -V_{SS} + V_{CS} + V_t + V_{OV}$ where V_{CS} is the required voltage of current source I

The differential pair responds to differential input signals: $v_{id} = v_{GS1} - v_{GS2}$
Range of differential-mode operation: $-\sqrt{2}V_{OV} \le v_{id} \le \sqrt{2}V_{OV}$
The current I can be steered from one transistor to the other by varying v_{id} in the range.
To use the differential pair as a linear amplifier, we keep the differential input signal v_{id} small.



$$i_{D1} = \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2}$$

$$i_{D2} = \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)\sqrt{1 - \left(\frac{v_{id}/2}{V_{OV}}\right)^2}$$

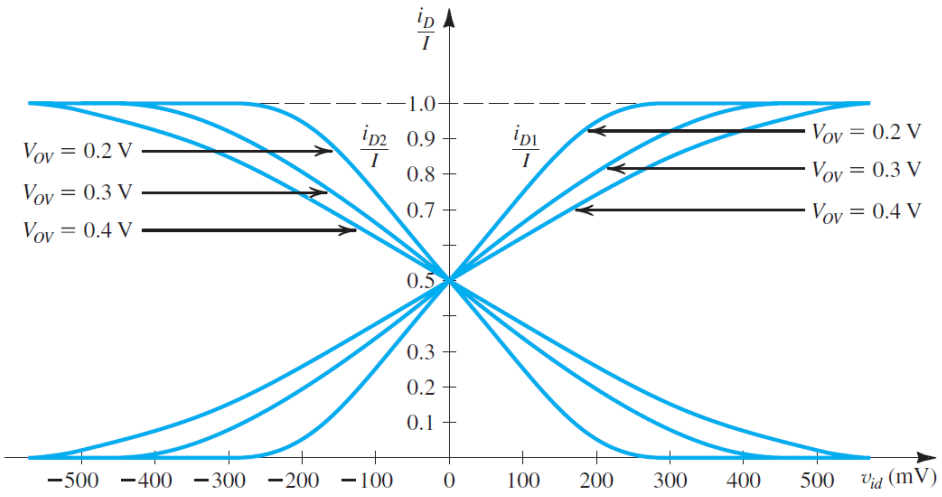
$where\ v_{id} = v_{G1} - v_{G2}$

The transfer characteristics is nonlinear due to the term involving v_{id}^2 to obtain linear amplification keep $v_{id}/2 \ll V_{OV}$. So:

$$\boldsymbol{i_{D1} \simeq \frac{I}{2} + \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)}$$

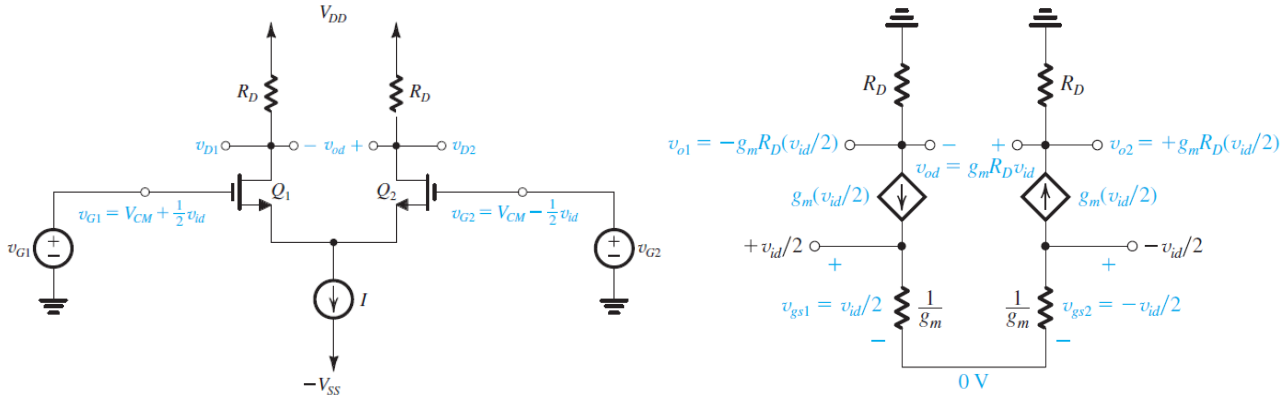
$$\boldsymbol{i_{D2} \simeq \frac{I}{2} - \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)}$$

$$i_d = \left(\frac{I}{V_{OV}}\right)\left(\frac{v_{id}}{2}\right)$$



Linearity can be increased by increasing the overdrive voltage V_{OV}, done by using smaller W/L. The price paid for the increased linearity is a reduction in g_m and hence a reduction in gain.
I can be increased to obtain a higher g_m. The expense for doing this is increased power dissipation, a serious limitation in IC design.

Small-Signal Operation:



V_{CM} denotes a common-mode dc voltage, typically the middle value of the power supply.
The differential input signal v_{id} is applied in a complementary v_{G1} is increased by $v_{id}/2$ and v_{G2} is decreased by $v_{id}/2$.

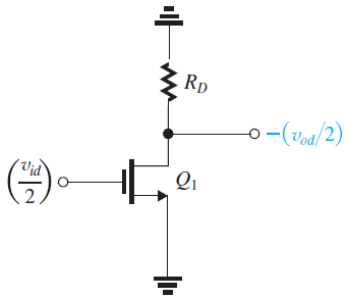
$$\boldsymbol{g_m = \frac{2I_D}{V_{OV}} = \frac{I}{V_{OV}}}$$

Output can be taken either between one of the drains and ground or between the two drains.

- Single-ended outputs $v_{o1} = -g_m \frac{v_{id}}{2} R_D \quad v_{o2} = +g_m \frac{v_{id}}{2} R_D$
  - $\boldsymbol{\frac{v_{o1}}{v_{id}} = -\frac{1}{2} g_m R_D}$
  - $\boldsymbol{\frac{v_{o2}}{v_{id}} = +\frac{1}{2} g_m R_D}$
- Differential output $v_{od} = v_{o2} - v_{o1}$
  - **Differential Gain:** $\boldsymbol{A_d = \frac{v_{od}}{v_{id}} = g_m R_D}$

Differential Half-Circuit: when a symmetrical differential amplifier is fed with a differential signal in a balanced manner the performance can be determined by considering only half the circuit.
A_d can be determined directly from the half-circuit.

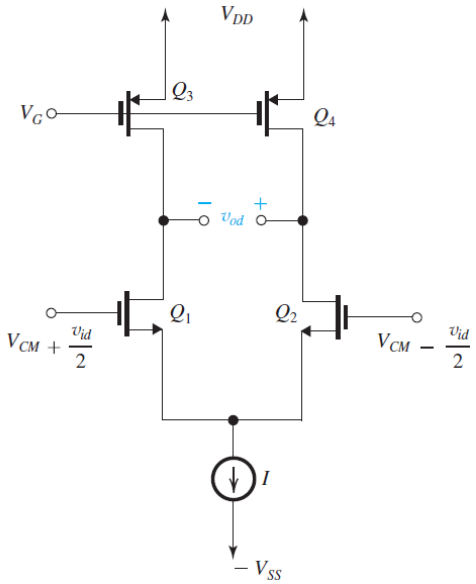
$$\boldsymbol{A_d = g_m(R_D \| r_o)}$$



Differential Amplifier with Current-Source Loads: to obtain higher gain, the passive resistances R_D can be replaced with current sources.

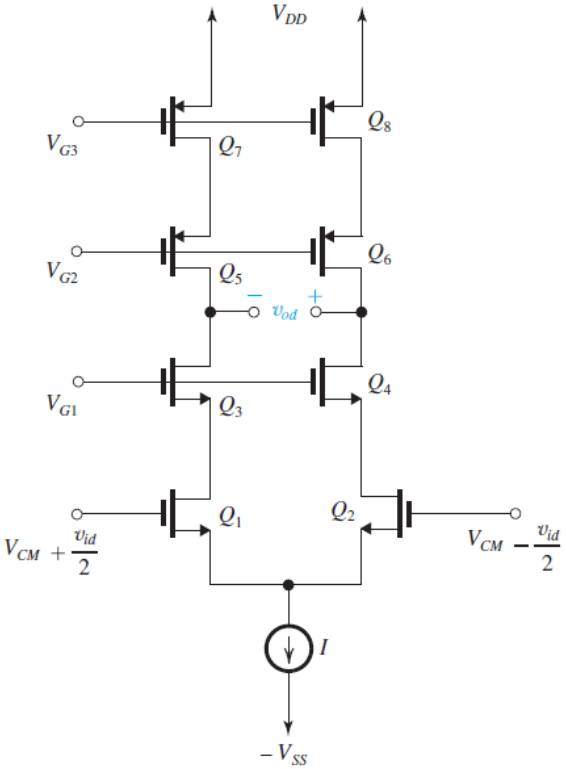
$$A_d = \frac{v_{od}}{v_{id}} = g_{m1}(r_{o1} \| r_{o3})$$

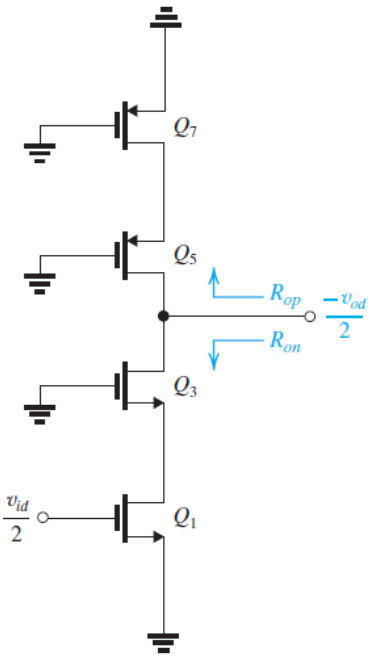
Example with current-source loads formed by Q_3 and Q_4:



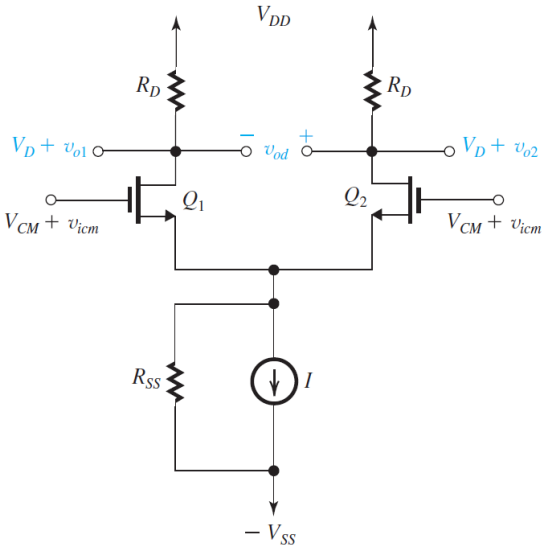
Cascode Differential Amplifier: the gain of the differential amplifier can be increased by utilizing this configuration. $\boldsymbol{A_d = \frac{v_{od}}{v_{id}} = g_{m1}(R_{on} \| R_{op})}$

where $R_{on} = (g_{m3}r_{o3})r_{o1}$ and $R_{oo} = (g_{m5}r_{o5})r_{o7}$





7.2. Common-Mode Rejection



Differential amplifier responds to a differential input signal and completely rejects a common-mode signal. Changes in V_{CM} over a wide range result in no change in the voltage at either of the two drains. In a realistic situation of the current source having a finite output resistance, the common-mode gain will no longer be zero.

R_{SS} has the effect on the bias current of Q_1 and Q_2 that will no longer be $I/2$ but will be larger than $I/2$. However, since $\boldsymbol{R_{SS}}$ **is usually very large**, this additional dc current is usually small and we shall neglect it, thus assuming that Q_1 and Q_2 continue to operate at a bias current of $I/2$.

R_{SS} has no effect on the value of A_d.

v_{o1} and v_{o2} will be corrupted by the common-mode signal v_{icm}: $\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \simeq -\frac{R_D}{2R_{SS}}$

The differential output voltage v_{od} will remain free of common-mode interference $v_{od} = 0$.

The circuit still rejects common-mode signals, but this will not be the case if the circuit is not perfectly symmetrical.

Effect of R_D Mismatch: when the two drain resistances exhibit a mismatch ΔR_D the common-mode voltages at the two drains will no longer be equal. The load of Q_1 is R_D and of Q_2 is $(R_D + \Delta R_D)$.

- $v_{o1} \simeq -\frac{R_D}{2R_{SS}} v_{icm}$
- $v_{o2} \simeq -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm}$
- $\boldsymbol{A_{cm} = \frac{v_{od}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}} = -\left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right)}$

Thus, a portion of the interference or noise signal v_{icm} will appear as a component of v_{od}. A measure of the effectiveness of the differential amplifier is the common-mode rejection ratio (CMRR).

$$\boldsymbol{CMRR = \frac{|A_d|}{|A_{cm}|} = (2g_m R_{SS}) / \left(\frac{\Delta R_D}{R_D}\right)}$$

We want CMRR high.

Effect of g_m Mismatch on CMRR:

- $\Delta g_m = g_{m1} - g_{m2}$
- $A_{cm} \simeq \left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta g_m}{g_m}\right)$
- $\boldsymbol{CMRR = (2g_m R_{SS}) / \left(\frac{\Delta g_m}{g_m}\right)}$

To keep CMRR high use a biasing current source with a high output resistance R_{SS}.

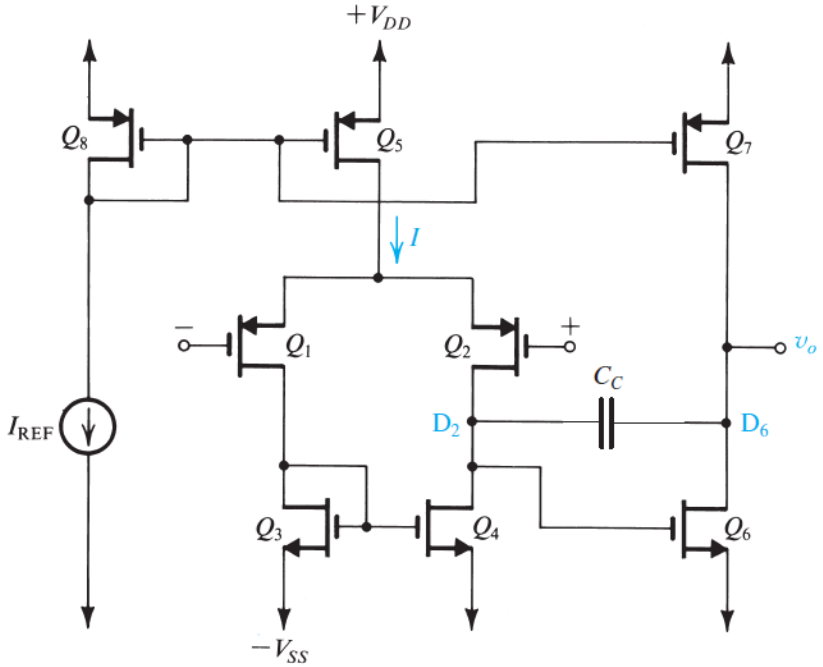
Differential versus Single-Ended Output: taking the output single-endedly will CMRR is reduced dramatically. So, to obtain a large CMRR, the output of the differential amplifier must be taken differentially.

7.3. Multistage Amplifiers

Practical transistor amplifiers usually consist of a number of stages connected in cascade.

- The **first (or input) stage** is usually required to provide a high input resistance in order to avoid loss of signal.
  In a differential amplifier the input stage must also provide large common-mode rejection.
- The function of the **middle stages** is to provide the bulk of the voltage gain. Other functions are the conversion of the signal from differential mode to single-ended mode and the shifting of the dc level of the signal in order to allow the output signal to swing both positive and negative.
- The main function of **the last (or output) stage** is to provide a low output resistance in order to avoid loss of gain when a low-valued load resistance is connected.
  Also, should be able to supply the current required by the load in an efficient manner—that is, without dissipating an unduly large amount of power in the output transistors.

A Two-Stage CMOS Op Amp: a popular structure for CMOS utilizes two power supplies, which can range from ±2.5 V for the 0.5-μm technology down to ±0.5 V for the 65-nm technology. A reference bias current I_{REF} is generated either externally or using on-chip circuits.
The current mirror formed by Q8 and Q5 supplies the differential pair Q1–Q2 with bias current.
The input differential pair is actively loaded with the current mirror formed by Q3 and Q4.
The second stage consists of Q6, which is a common-source amplifier loaded with the current-source transistor Q7.
A striking feature of the circuit is that it does not have a low-output-resistance stage.
The output resistance of the circuit is equal to $(r_{o6} \| r_{o7})$.
This circuit is not suitable for driving low-impedance loads.
The circuit is very popular and is used frequently for implementing op amps in VLSI circuits, where the op amp needs to drive only a small capacitive load.
First stage Voltage gain: $A_1 = -g_{m1}(r_{o2} \| r_{o4})$
Second stage Voltage gain: $A_2 = -g_{m6}(r_{o6} \| r_{o7})$
The dc open loop gain of the op amp is the product of A_1 and A_2.

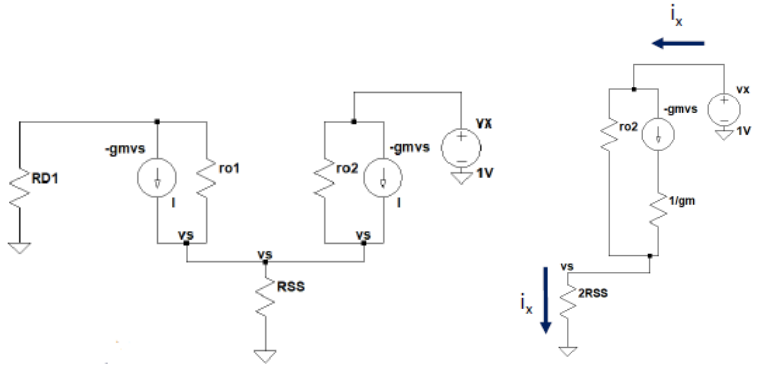


Esame

Amplificatore con resistenza Rss al source:

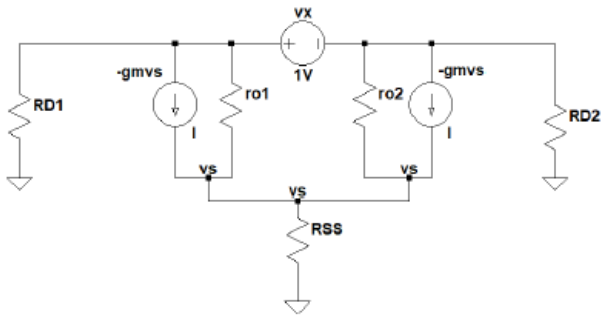
- Calcolo punto di lavoro: si impone $V_{CM} = v_{G1} = v_{G2} = 0$
- Calcolo $r_o = 1/\lambda$ e $g_m = k_n(V_{GS} - V_T)$
- $\boldsymbol{A_d(single)} = \frac{\boldsymbol{g_m(R_D \| r_o)}}{\boldsymbol{2}}$ $\quad A_{cm} = \frac{g_m R_D}{1+2g_m R_{SS}}$
- $\boldsymbol{CMRR} = \frac{|\boldsymbol{A_d}|}{|\boldsymbol{A_{cm}}|} \simeq \boldsymbol{g_m R_{SS}}$
- Resistenza uscita single ended:

Rout (senza RD) = (1 + 2 gmRss)ro2 + 2Rss
Rout (con RD) = [(1 + 2 gmRss)ro2 + 2Rss]//RD



- Resistenza uscita differenziale:

$$i_x = g_m v_s + i_{r_{o1}}$$
$$i_x = g_m v_s + i_{r_{o2}}$$
$$i_{r_{o1}} = -i_2$$
$$r_o = 2(\boldsymbol{R_D \| r_o})$$



Amplificatore con generatore di corrente:

- Calcolo punto di lavoro: si impone $V_{CM} = v_{G1} = v_{G2} = 0$
- $I_{D1} = I_{D2} = I/2$
- $V_{OV} = \sqrt{I/k_n}$
- $g_m = k_n(V_{GS} - V_T)$
- $\boldsymbol{A_d(single)} = \frac{\boldsymbol{g_m(R_D \| r_o)}}{\boldsymbol{2}}$ $\quad A_{cm} = \frac{g_m R_D}{1+2g_m R_{SS}} = 0$

Amplificatore con generatore di corrente//Rss:

- $v_{od} = 0$
- $\boldsymbol{A_d(single)} = \mp\frac{\boldsymbol{g_m(R_D \| r_o)}}{\boldsymbol{2}}$
- $A_{cm} = \frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \simeq -\frac{R_D}{2R_{SS}}$
- $\boldsymbol{A_d = g_m(R_D \| r_o)}$

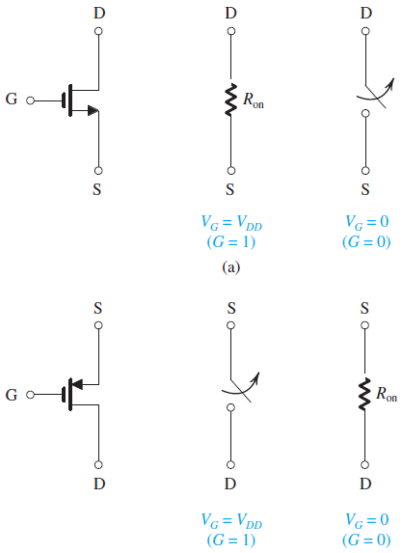
Amplificatore differenziale con generatore di corrente current mirror:

- Si calcola la corrente del current mirror con i W e L opportuni

8.CMOS Digital Logic Circuits

8.1. CMOS Logic-Gate Circuits

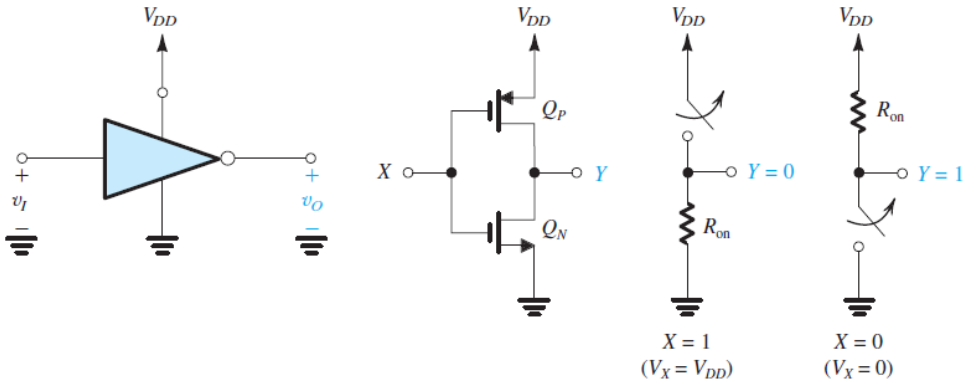
In combinational circuits, the output at any time is a function only of the values of input signals at that time. These circuits do not have memory and do not employ feedback.



Switch-Level Transistor Model: CMOS digital circuits utilize NMOS and PMOS transistors operating as switches. A MOS transistor can operate as an on/off switch in the triode region ("on" position) and in the cutoff region ("off" position).

NMOS transistor behaves as a closed switch, exhibiting a very small resistance (R_{on} or r_{DS}) between its drain and source terminals when its gate voltage is high. When the gate voltage is low the transistor is cut off.

CMOS Inverter:



General Structure of CMOS Logic consists of two networks:

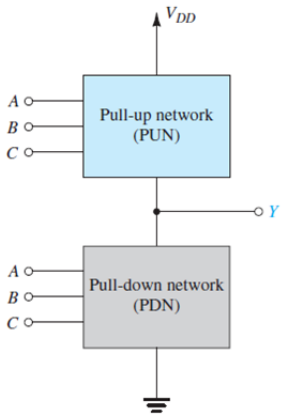
- the **pull-down** network (PDN) constructed of **NMOS** transistors
- the **pull-up** network (PUN) constructed of **PMOS** transistors.

The two networks are operated by the input variables.

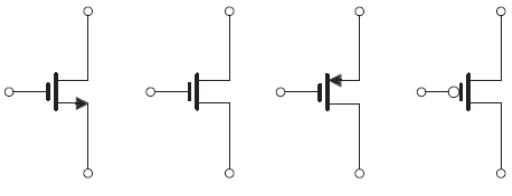
PDN will conduct for all input combinations that require a low output (Y = 0) and will then pull the output node down to ground, simultaneously the PUN will be off.

All input combinations that call for a high output (Y = 1) will cause the PUN to conduct, and the PUN will then pull the output node up to V_{DD}.

PDN utilizes devices in parallel to form an OR function and devices in series to form an AND function.



Alternative circuit symbols that are almost universally used:



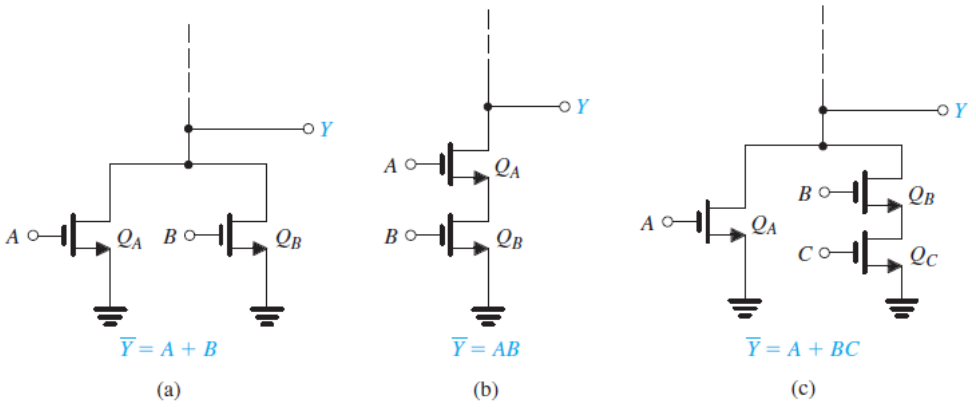


Figure 14.4 Examples of pull-down networks.

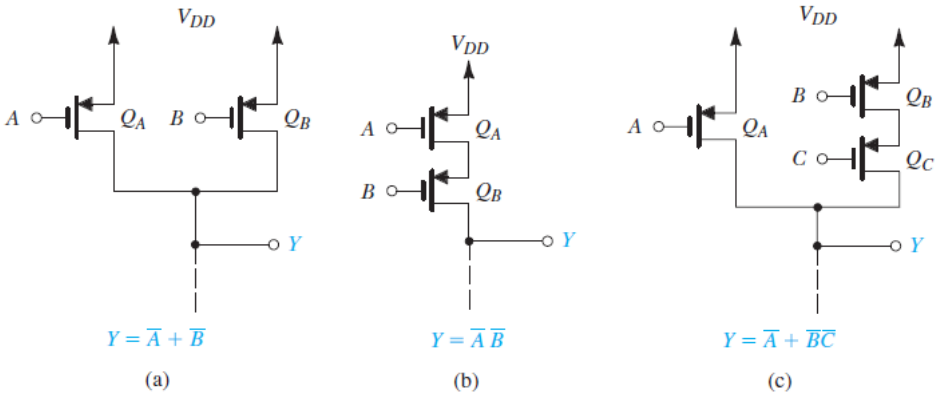
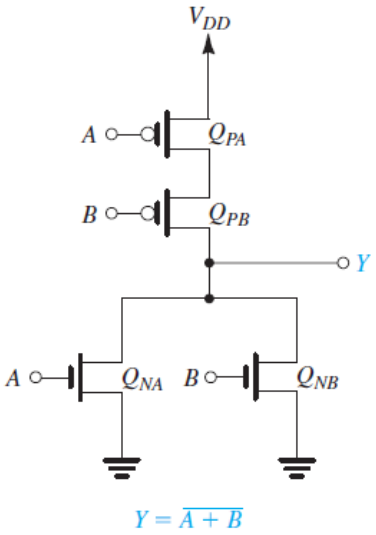


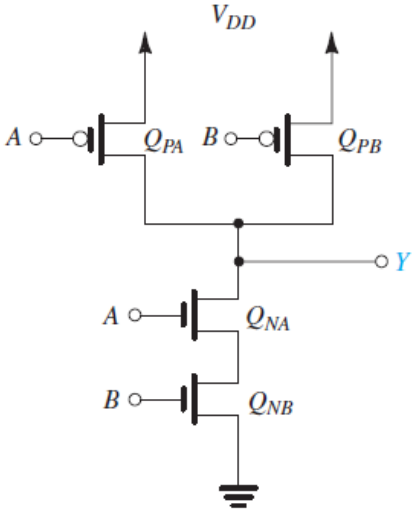
Figure 14.5 Examples of pull-up networks.

The Two-Input NOR Gate:

Extension to a higher number of inputs: for each additional input, an NMOS transistor is added in parallel with Q_{NA} and Q_{NB}, and a PMOS transistor is added in series with Q_{PA} and Q_{PB}.

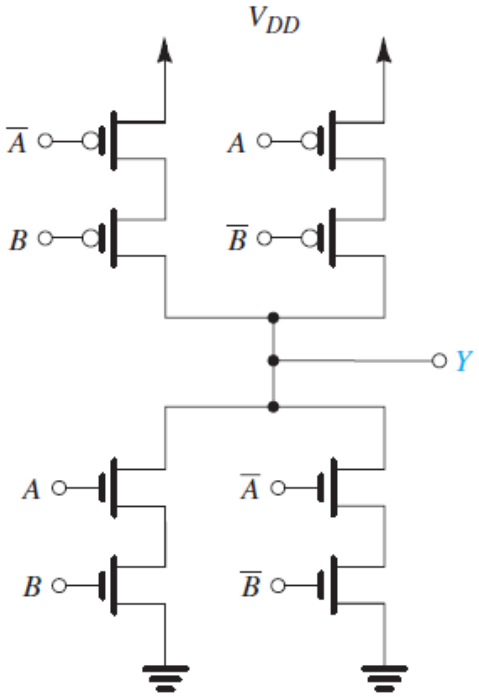


The Two-Input NAND Gate: $Y = \overline{AB} = \bar{A} + \bar{B}$



Obtaining the PUN from the PDN and Vice Versa: where a series branch exists in one, a parallel branch exists in the other.

The Exclusive-OR Function: $Y = A\bar{B} + \bar{A}B = AB + \bar{A}\bar{B}$. It's a non-symmetric network.

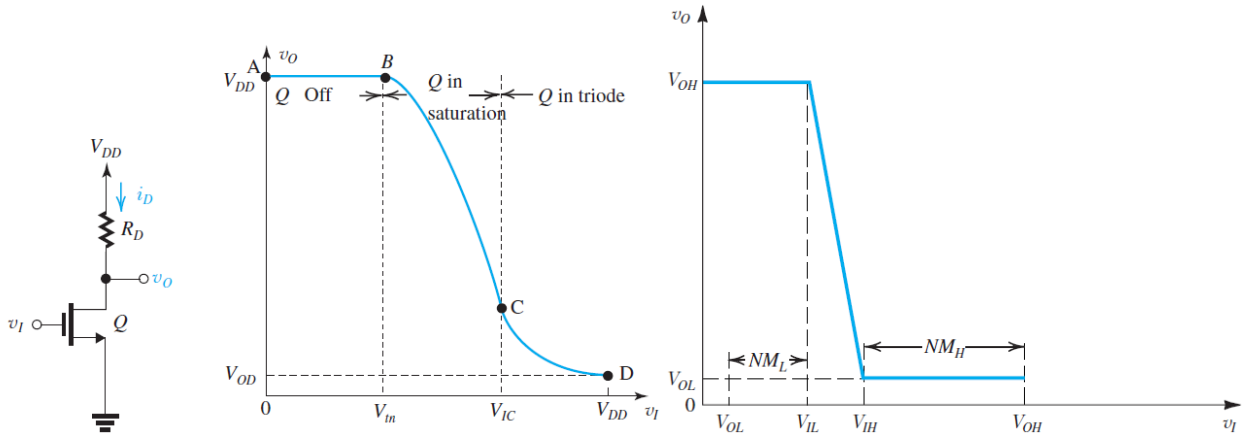


Synthesis of a function:

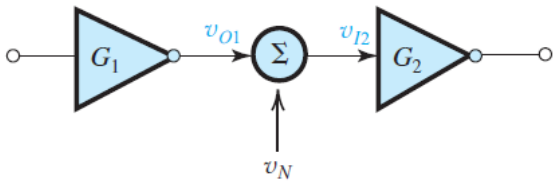
- Express the function in the negative form
- Remove the negation sign and synthesize the **pull-down** network:
  - OR (+): NMOS in parallel
  - AND (x): NMOS in series
- Pull-up, from pull-down:
  - NMOS --> PMOS
  - Parallel --> Series
  - Series --> Parallel

8.2. Digital Logic Inverters

The Voltage-Transfer Characteristic (VTC): to use this amplifier as a logic inverter, we utilize its extreme regions of operation. This is exactly the opposite to its use as a signal amplifier, where it would be biased at the middle of the transfer characteristic.

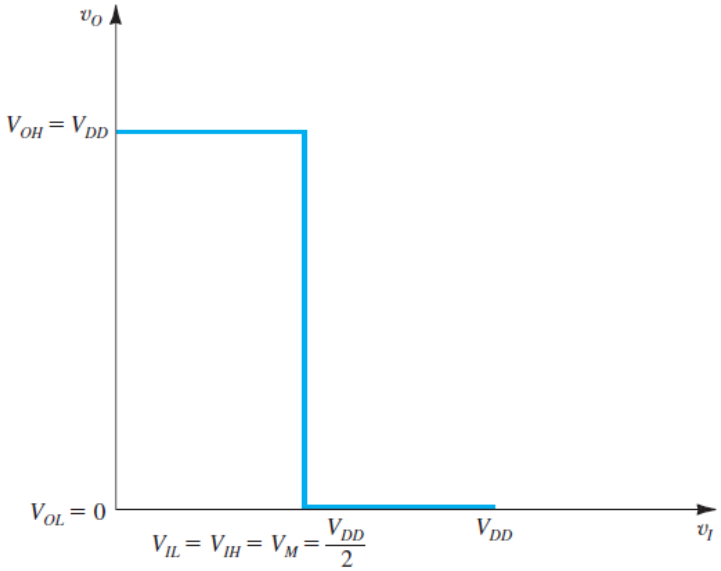


Noise Margins: a noise or interference signal v_N is somehow coupled to the interconnection between the output of inverter G1 and the input of inverter G2.



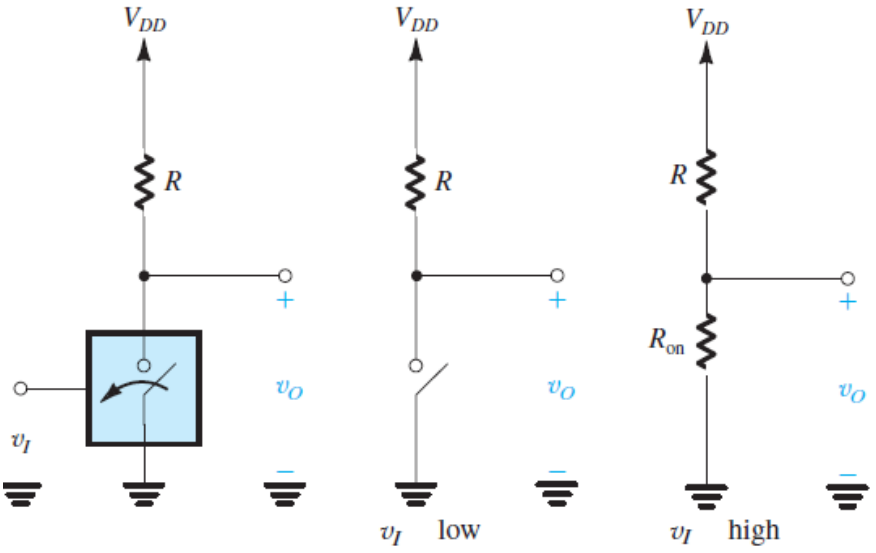
Input of G2: $v_{I2} = v_{O1} + v_N$
Output low level V_{OL}
Output high level V_{OH}
V_{IL} Maximum value of input interpreted by the inverter as a logic 0
V_{IH} Minimum value of input interpreted by the inverter as a logic 1
Low input noise margin $NM_L = V_{IL} - V_{OL}$
High input noise margin $NM_H = V_{OH} - V_{IH}$

Ideal VTC: when $V_{OH} = VDD$ and $V_{OL} = 0$ CMOS technology come very close to realizing the ideal VTC.

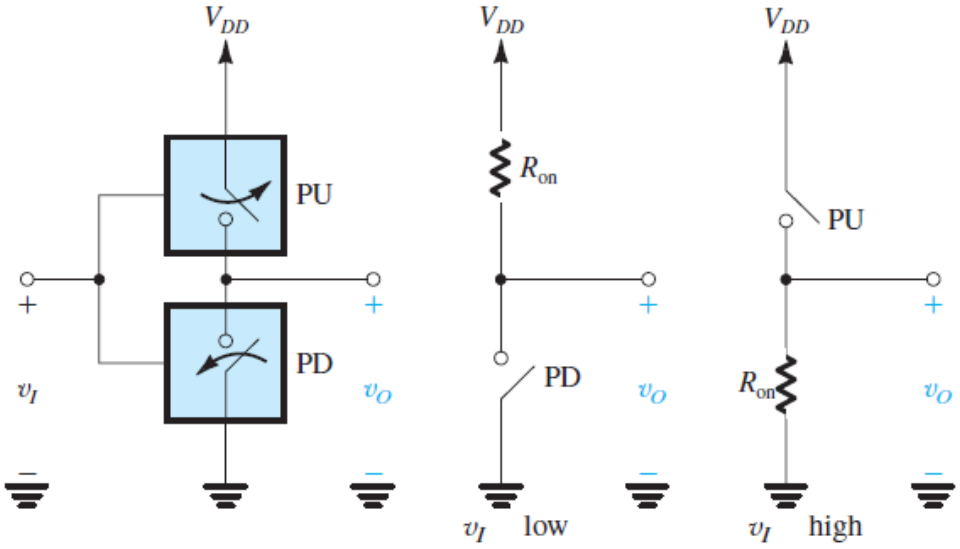


Inverter implementation as voltage-controlled switches: when v_I is low, the switch will be open and $v_O = V_{DD}$, since no current flows through R. When v_I is high, the switch will be closed and, assuming an ideal switch, v_O will be 0.
Although their off-resistances are very high the "on" switch has a finite on-resistance R_{on}.

$$V_{OL} = V_{DD}\frac{R_{on}}{R + R_{on}}$$



More elaborated implementation:



8.3. The CMOS Inverter

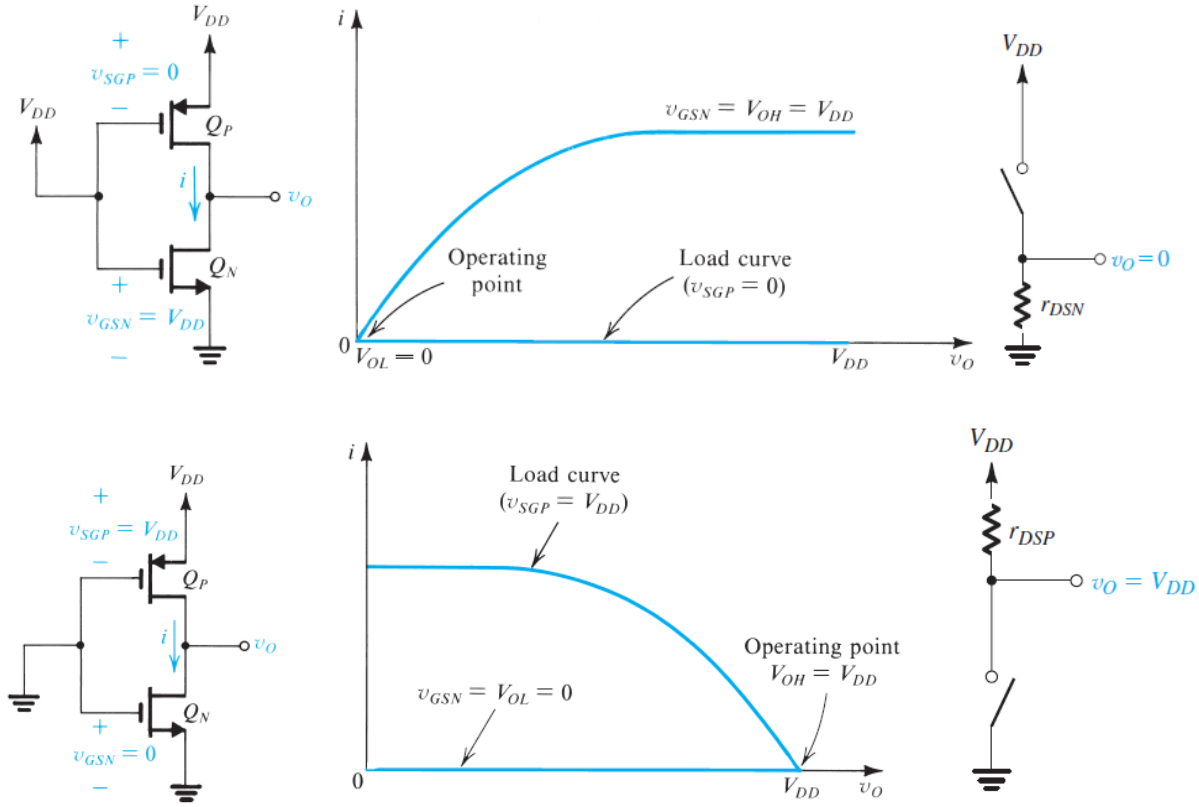
Circuit Operation:

- when $v_I = V_{DD}$: QN provides a low-resistance path between the output terminal and ground

$$r_{DSN} = 1/\left[k'_n \left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})\right]$$

- when $v_I = 0$: QP provides a low-resistance path between the output terminal and V_{DD}

$$r_{DSP} = 1/\left[k'_n \left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)\right]$$



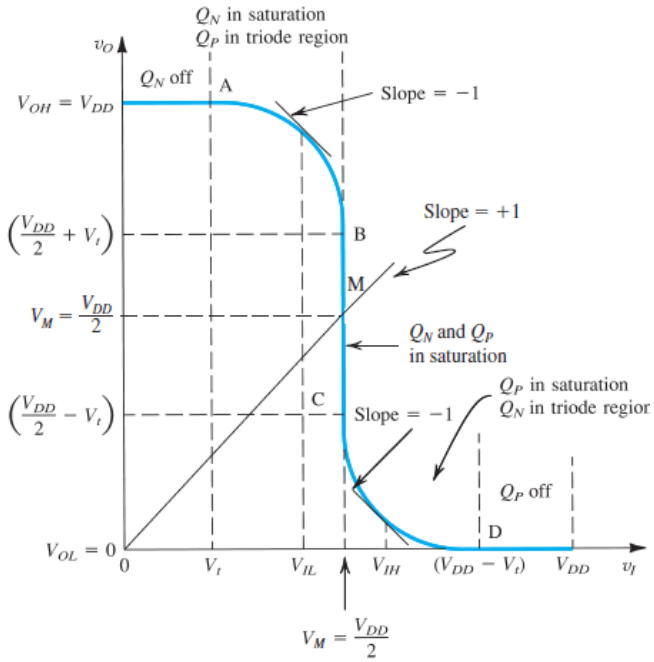
The basic CMOS logic inverter behaves as an ideal inverter. In summary:

- The output voltage levels are 0 and V_{DD}
- static power dissipation in the inverter is zero in both of its states
- A low-resistance path exists between the output terminal and ground or V_{DD}.
  These low-resistance paths ensure that the output voltage is 0 or V_{DD}
- The low output resistance makes the inverter less sensitive to the effects of noise and other disturbances.
- The input resistance of the inverter is infinite (because $I_G = 0$). Thus the inverter can drive an arbitrarily large number of similar inverters with no loss in signal level.

The Voltage-Transfer Characteristic (VTC):

For Q_N: $i_{DN} = \begin{cases} k_n'\left(\frac{W}{L}\right)_n\left[(v_I - V_{tn})v_O - \frac{1}{2}v_O^2\right], & \text{for } v_O \le v_I - V_{tn} \\ \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(v_I - V_{tn})^2, & \text{for } v_O \ge v_I - V_{tn} \end{cases}$

For Q_P: $i_{DP} = \begin{cases} k_p'\left(\frac{W}{L}\right)_p\left[(V_{DD} - v_I - |V_{tp}|)(V_{DD} - v_O) - \frac{1}{2}(V_{DD} - v_O)^2\right], & \text{for } v_O \ge v_I + |V_{tp}| \\ \frac{1}{2}k_p'\left(\frac{W}{L}\right)_p(V_{DD} - v_I - |V_{tp}|)^2, & \text{for } v_O \le v_I + |V_{tp}| \end{cases}$



When Q_N and Q_P are matched:

- $V_{tn} = |V_{tp}| = V_t$
- $k_n'\left(\frac{W}{L}\right)_n = k_p'\left(\frac{W}{L}\right)_p$
- $\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$

$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$

$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$

$NM_H = \frac{1}{8}(3V_{DD} + 2V_t)$

$NM_L = \frac{1}{8}(3V_{DD} + 2V_t)$

When Q_N and Q_P are NOT matched: the price paid for obtaining a perfectly symmetric VTC is that the width of the p-channel device can be three to four times as large as that of the n-channel device. This can result in a relatively large silicon area.

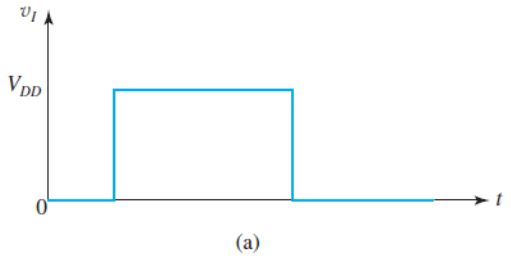
$$V_M = \frac{r(V_{DD} - |V_{tp}|) + V_{tn}}{r + 1} \quad \text{where } r = \sqrt{k_p/k_n}$$

Q_N and Q_P have the same channel length L.

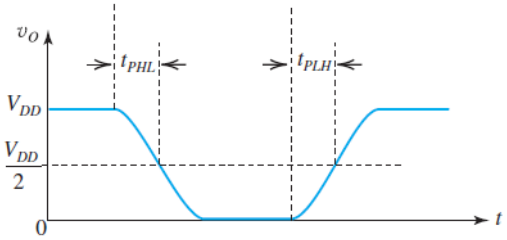
8.4. Dynamic Operation of the CMOS Inverter

The speed of operation of a digital system (e.g., a computer) is determined by the propagation delay of the logic gates used to construct the system.

Propagation Delay: the output signal has rounded edges. There is a time delay between each edge of the input pulse and the corresponding change in the output of the inverter. there are two propagation delays, which are not necessarily equal: the propagation delay for the output going from high to low, t_{PHL}, and the propagation delay for the output going from low to high, t_{PLH}.



(a)



Inverter propagation delay $t_p = \frac{1}{2}(t_{PLH} + t_{PHL})$

Maximum switching frequency $f_{max} = \frac{1}{T_{min}} = \frac{1}{2t_P}$

fundamental relationship in analyzing the dynamic operation of a circuit is: $I\Delta t = \Delta Q = C\Delta V$

current I flowing through a capacitance C for an interval Δt deposits a charge ΔQ on the capacitor, which causes the capacitor voltage to increase by ΔV.

Determining the Propagation Delay of the CMOS Inverter: replace all the capacitances in the circuit with a single equivalent capacitance C connected between the output node of the inverter and ground. Assuming $\lambda_n = 0$

- $t_{PHL} = \frac{\alpha_n C}{k'_n (W/L)_n V_{DD}}$ where $\alpha_n = 2/\left[\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2\right]$ $= [1 \div 2]$
- $t_{PLH} = \frac{\alpha_p C}{k'_p (W/L)_p V_{DD}}$ where $\alpha_p = 2/\left[\frac{7}{4} - \frac{3|V_{tn}|}{V_{DD}} + \left|\frac{V_{tn}}{V_{DD}}\right|^2\right]$ $= [1 \div 2]$
- $t_p = \frac{1}{2}(t_{PHL} + t_{PLH})$

t_p is proportional to C, the designer should strive to reduce C. This is achieved by using the minimum possible channel length and by minimizing wiring and other parasitic capacitances.

With larger transconductance parameter k' can result in shorter propagation delays.

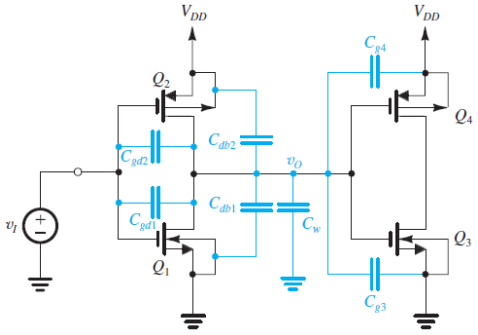
A larger W/L ratios can result in a reduction in t_p

A larger supply voltage V_{DD} results in a lower t_p

Alternative approach:

- $\boldsymbol{t_{PHL} = 0.69 R_n C \simeq R_n C}$ where $R_n = \frac{12.5}{(W/L)_n} k\Omega$
- $\boldsymbol{t_{PLH} = 0.69 R_p C \simeq R_p C}$ where $R_p = \frac{30}{(W/L)_p} k\Omega$

Determining the Equivalent Load $C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$



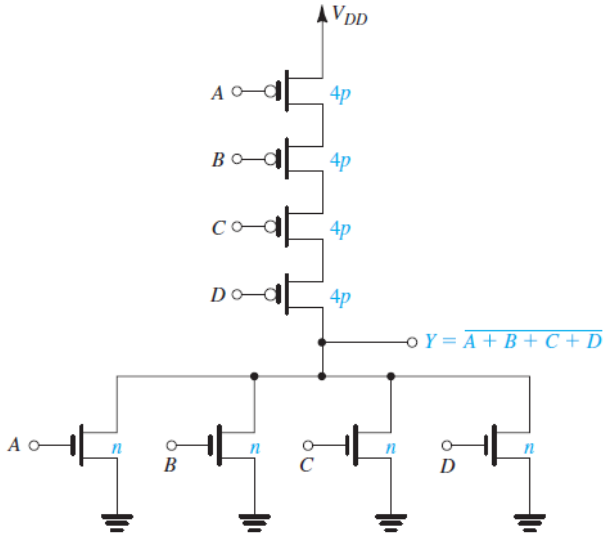
8.5. Transistor Sizing

Inverter Sizing: to minimize area, the length of all channels is usually made equal to the minimum length permitted by the given technology.
If our interest is strictly to minimize area, $(W/L)_n$ is usually selected in the range 1 to 1.5.
The selection of $(W/L)_p$ relative to $(W/L)_n$ has influence on the noise margins and t_{PLH}.
Selecting $(W/L)_p = (W/L)_n$ is a possibility, and $(W/L)_p = 2(W/L)_n$ is a frequently used compromise.

- $R_{eq} = \frac{1}{2}(R_N + R_P)$
- $t_p = 0.69\left(\frac{R_{eq0}}{S}\right)(SC_{int0} + C_{ext})$ *where S is scaling factor*

Transistor Sizing in CMOS Logic Gates: for the basic inverter design, denote $(W/L)_n = n$ and $(W/L)_p = p$, where n is usually 1 to 1.5 and, for a matched design, $p = (\mu\_n/\mu\_p\,)n$. Often $p = 2n$.
Select individual W/L ratios for all transistors in a logic gate so that the PDN should be able to provide a capacitor discharge current at least equal to that of an NMOS transistor with $W/L = n$, and the PUN should be able to provide a charging current at least equal to that of a PMOS transistor with $W/L = p$. This will guarantee a worst-case gate delay equal to that of the basic inverter.
Worst case: means that in deciding on device sizing, we should **find the input combinations that result in the lowest output current** and then choose sizes that will make this current equal to that of the basic inverter.
Find the equivalent W/L ratio of a network of MOS transistors by considering the parallel and series connection of MOSFETs and find the equivalent W/L ratios.

- MOSFETs in **series:** $\boldsymbol{(W/L)_{eq} = \frac{1}{\frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \cdots}}$
- MOSFETs in **parallel:** $\boldsymbol{(W/L)_{eq} = (W/L)_1 + (W/L)_2 + \cdots}$

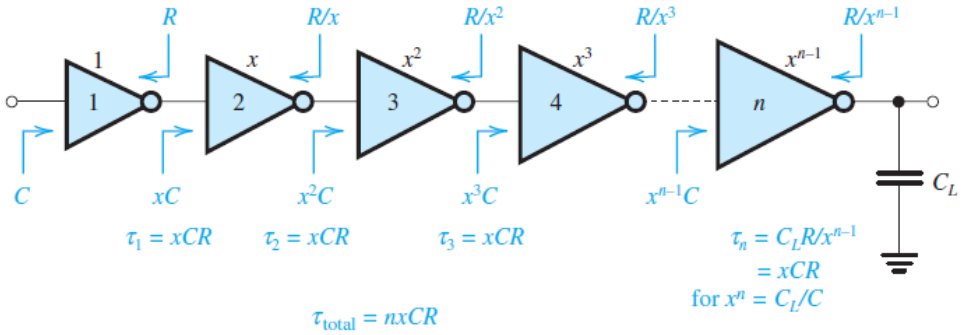


Example:

- PDN worst case: just 1 MOS conducting
  --> $(W/L)_{eq} = \frac{1}{\frac{1}{(W/L)_1}} = n$
- PUN worst case: 4 MOS conducting
  --> $(W/L)_{eq} = (W/L)_1 + \cdots + (W/L)_4 = 4p$

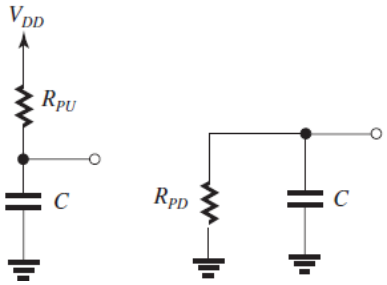
Effects of Fan-In and Fan-Out on Propagation Delay: each additional input to a CMOS gate requires two additional transistors, one NMOS and one PMOS.
The additional transistor in CMOS not only increases the chip area but also increases the total effective capacitance per gate and in turn increases the propagation delay. Although CMOS has many advantages, it does suffer from increased circuit complexity when the fan-in(chip area) and fan-out(propagation delay) are increased.

Driving a Large Capacitance: in many cases a logic gate must drive a large load capacitance. This might, for example, be due to a long wire on a chip. How to drive such a large load capacitance without causing the propagation delay to be unacceptably large?
Having an output resistance R, the propagation delay $t_p = \tau = C_L R$ can be very large.
To reduce the propagation delay, we can make the driver inverter m times larger than the standard inverter. Its output resistance will be R/m, $t_p = C_L R/m$. However, the input capacitance of the large inverter is mC, which can be very large.
A chain of inverters connected in cascade n inverters of progressively larger sizes. each inverter in the chain is larger than the preceding inverter by the same factor x.
The delay time associated with the interface between each two succeeding inverters is $\tau = xCR$. Each interface contributes equally to the overall delay.
Overall delay $\boldsymbol{t_p = nxCR}$ $\quad x = [2.5 \div 4]$



8.6. Power Dissipation

A capacitance exists between the output node of the inverter and ground.



Dynamic power dissipation: as the inverter is switched from one state to another, current must flow through the switch(es) to charge (and discharge) the load capacitance. These currents give rise to power dissipation in the switches.

If the inverter is switched at a frequency of f Hz, the dynamic power dissipation of the inverter will be: $\boldsymbol{P_{dyn} = fCV_{DD}^2}$
To minimize the dynamic power dissipation, one must strive to reduce the value of C.
Peak current: $I_{peak} = \frac{1}{2} k_n \left(\frac{V_{DD}}{2} - V_{tm}\right)^2$

Power–Delay and Energy–Delay Products: one is usually interested in high-speed operation (low t_P) combined with low power dissipation. Unfortunately, these two requirements are often in conflict.
Power–delay product $\boldsymbol{PDP = P_D t_P = \frac{1}{2} CV_{DD}^2}$ is the energy consumed by the inverter for each output transition.
The lower the PDP, the more effective the inverter and the logic circuits based on the inverter are.
Although the PDP is a valuable metric for comparing different technologies for implementing inverters, it is not useful as a design parameter for optimizing a given inverter circuit.
A better metric is the **energy–delay product** $\boldsymbol{EDP = \text{Energy per transition} \times tP = \frac{1}{2} CV_{DD}^2 t_P}$